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MDC Connector & LED & SW	Page 31
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ATI RS690MC & SB600

MS-163B1

Version 0A

CPU:

AMD S1 638

System Chipset:
ATI RS690MC - North Bridge
ATI SB600 - South Bridge

On Board Chipset:
BIOS -- ISA EEPROM SHARE WITH EC/uP CONTROLLER
AUDIO -- REALTAK ALC883 AZALIA Audio CODEC
AMPLIFIER -- ANPEC APA2030 or TI TPA0212
KBC/EC/uP -- ENE3910
LAN -- MII PHY REALTEK RTL8101E
CLOCK -- ICS951462
1394 & Card Reader Controller -- REALTEK

Main Memory:
DDR II * 2 (Max 2GB)

Expansion Slots & Connector :
New Card X1
Mini-PCIE X1

MICRO-STAR INT'L CO.,LTD.

Title: COVER SHEET		
Size: Custom	Document Number: MS-163B1	Rev: 0A
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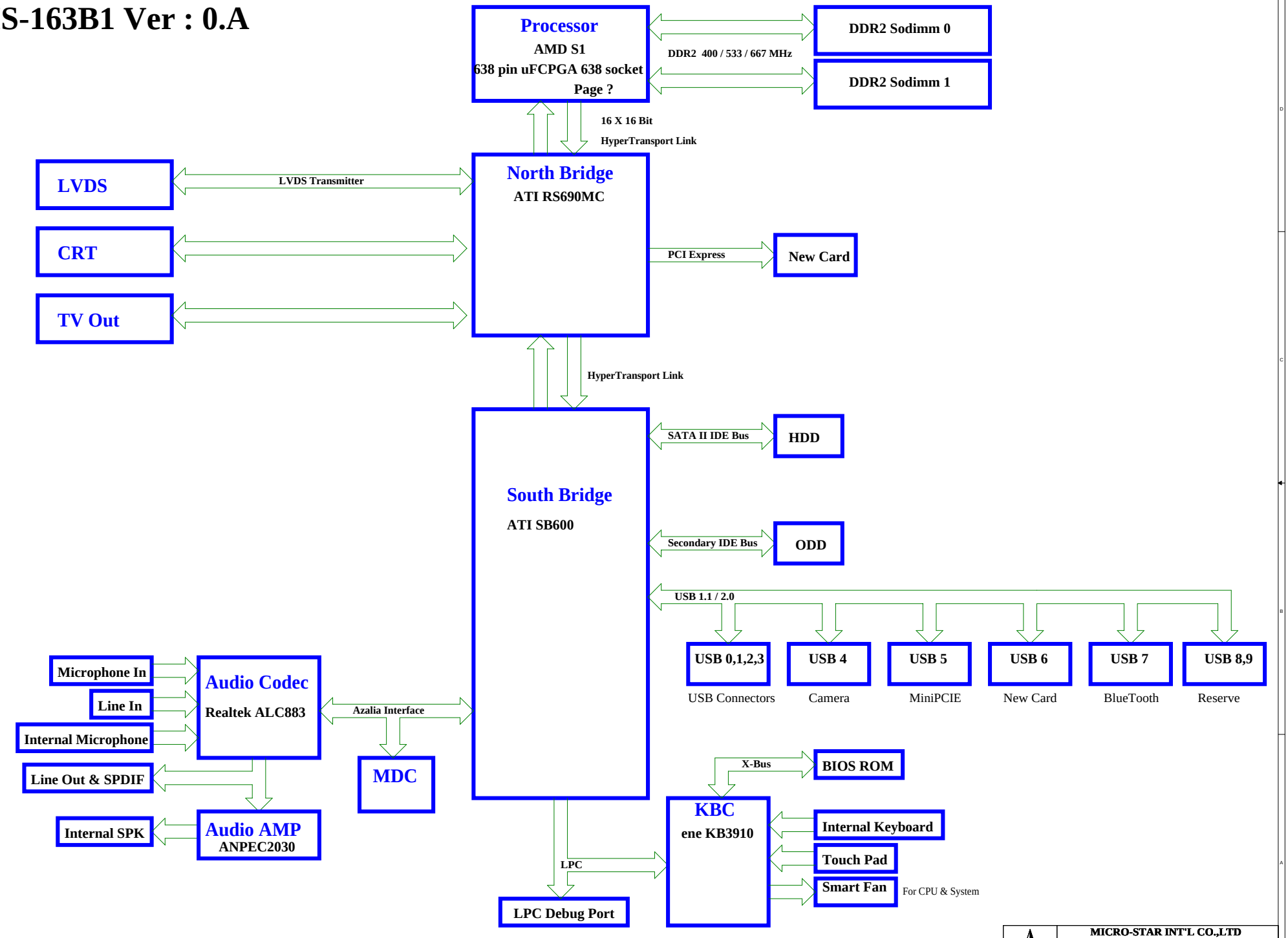

MICRO-STAR INT'L CO.,LTD	
MS-163B1	
Size: C	Document Description: Block Diagram
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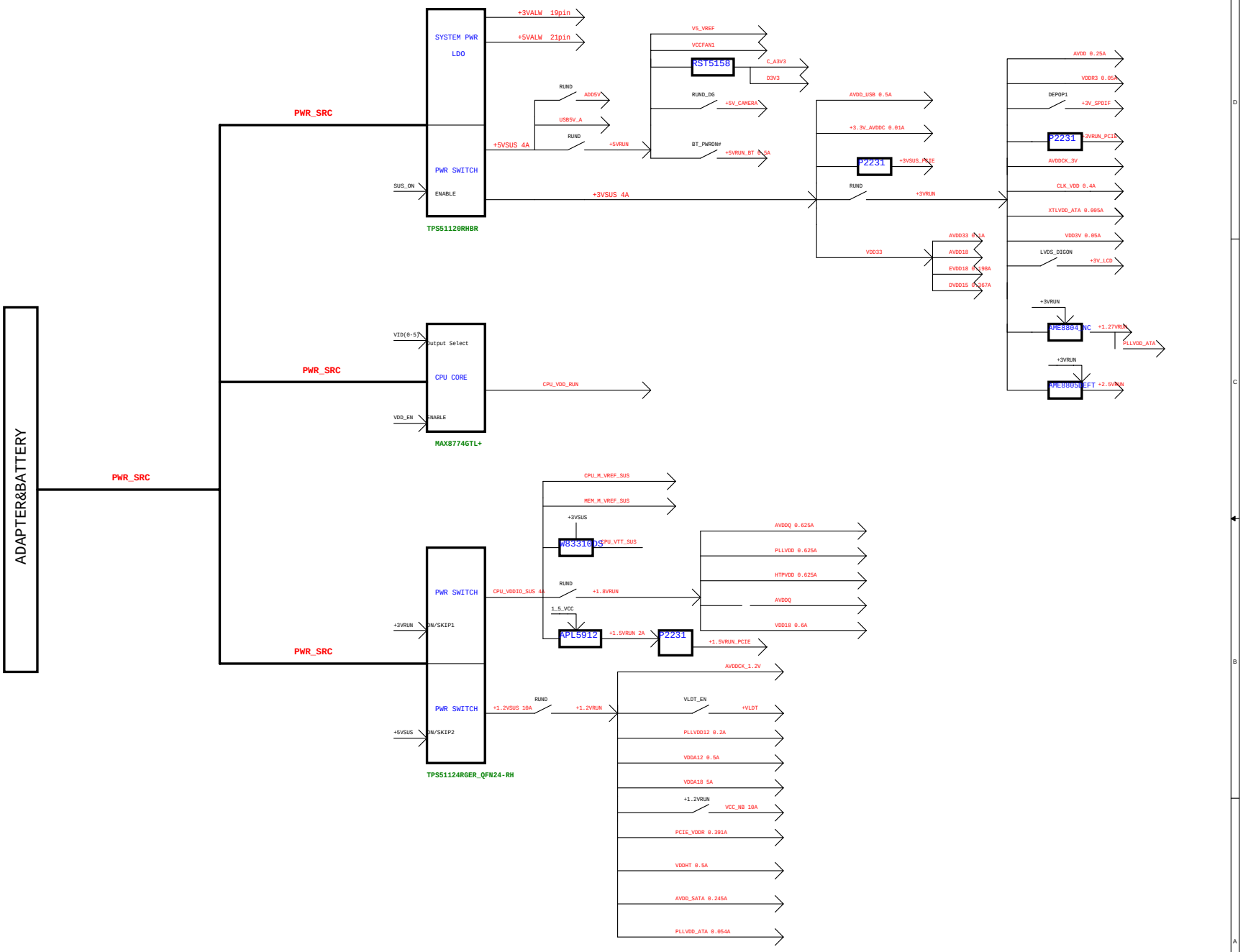
Date: Monday, April 23, 2007	Sheet 2 of 40



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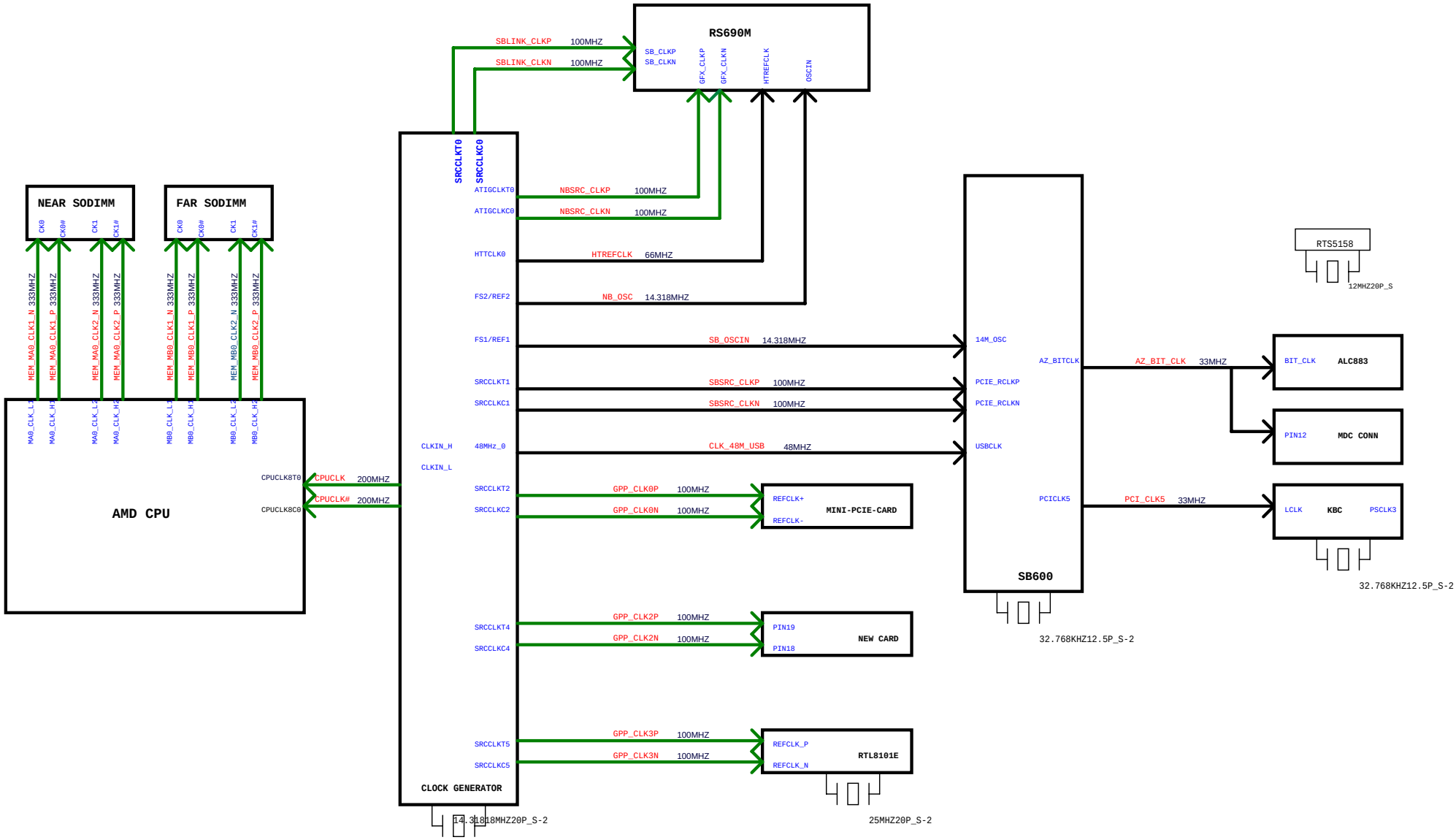
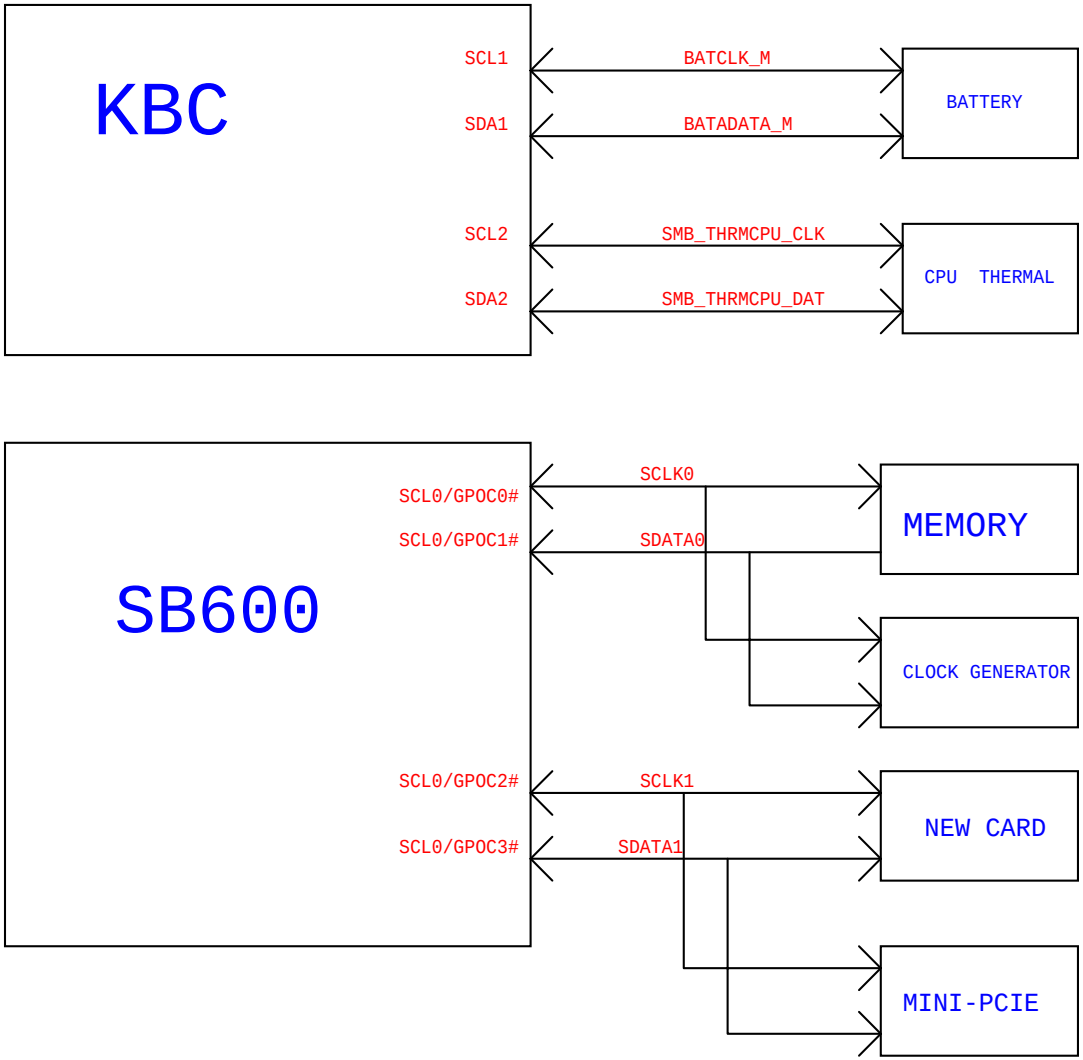
Size: Custom	Document Number: MS-163B1	Rev: 0A
Date: Monday, April 23, 2007	Sheet 3 of 40	



Title	CLOCK DISTRIBUTION		
Size B	Document Number MS-163B1		Rev 0A
Date: Monday, April 23, 2007	Sheet 4 of 40		



Title: I2C ILLUSTRATE		
Size: A	Document Number: MS-163B1	Rev: 0A
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ATHLON Control and Debug

LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

+VLDT
C262 C0.1U10X0402
C263 C0.1U10X0402
C264 C0.1U10X0402
C265 C0.1U10X0402

CPU_VDDA_2.5_RUN

+3VSUS
1u_6.3V_0402
PC2142
IN BP SHDN OUT GND
PU2007 RT9167/A
PC2140 0.01u_16V_0402
34 VDDA_EN
+VDDA
VDDA 2.5V
PC2139 10u_6V_0603
PD2007 S-RB751V-40
PR2121 1K_0402
PR2122 100K_0402
VDDA_PG
PC2138 2.2u_6V_0603
+VDDA
CP7 X_COPPER
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.
C260 C4.7U6.3X5S0805
C257 C0.1U10X0402
C256 C1000P50X0402
place them to CPU within 1"(5mil trace 10mil space)
+VLDT
R191 44.2R1% R188 44.2R1%
17 CPU_SIC_R 17 CPU_SID_R
CPU_HTREF1 CPU_HTREF0

U2D
VDDA2 VDDA1
PRESET_L PWROK LDTSTOP_L
SIC SID
HT_REF1 HT_REF0
VDD_FB_H VDD_FB_L
VDDIO_FB_H VDDIO_FB_L
CLKIN_H CLKIN_L
DBRDY DBREQ_L
TDI TDO TMS TCK TRST_L
TEST25_H TEST25_L TEST19 TEST18 TEST13 TEST9 TEST17 TEST16 TEST15 TEST14 TEST12 TEST7 TEST6 THERMDC THERMDA TEST3 TEST2
TEST29_H TEST29_L TEST24 TEST23 TEST22 TEST21 TEST20 TEST28_H TEST28_L TEST27 TEST26 TEST10 TEST8
RSVD0 RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14 RSVD15 RSVD16 RSVD17 RSVD18 RSVD19 RSVD20
MISC
AMD NPT S1 SOCKET Processor Socket

CPU_THERMTRIP# CPU_PROCHOT# 1.8
CPU_THERMTRIP_D# 18
CPU_VDDIO_SUS +1.8VRUN
R195 330R0402
R196 10KR0402
Q55 N-MMBT3904_NL_SOT23
CPU_VID5 CPU_VID4 CPU_VID3 CPU_VID2 CPU_VID1 CPU_VID0
CPU_PRESENT# TP14
CPU_SPI#_L
CPU_PSI# 37
Q54 N-MMBT3904_NL_SOT23
2/19 modify by benny
R192 10KR0402
R2038 510_0402 _NC
CPU_DBREQ#
CPU_TDO TP17
R219 80.6R1%0402
ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"
CPU_TEST29_H_FBCLKOUT_P
CPU_TEST29_L_FBCLKOUT_N
CPU_TEST21_SCANEN
CPU_TEST26_BURNIN#

CPU_VDDIO_SUS
CPUCLK C31 C3900P50X
CPU_CLKIN_SC_P CPU_CLKIN_SC_N
R14 169R1%0402 C32 C3900P50X
CPUCLK#
CPU_DBRDY TP21
TP15 CPU_TMS TP18 CPU_TCK TP16 CPU_TRST# TP19 CPU_TDI
R16 510R0402 R18 510R0402
CPU_TEST25_H_BYPASSCLK_H
CPU_TEST25_L_BYPASSCLK_L
CPU_TEST19_PLLTEST0
CPU_TEST18_PLLTEST1
CPU_TEST5_THERMDC CPU_TEST4_THERMDA
R287 X_10K_0402 +3VRUN
R274 X_4.7K_0402
CPU_PROCHOT# 1.8
Q23 X_SMBT3904
SB_TALERT# 19

RN20 8P4R-330R0402
CPU_SIC_R CPU_SID_R CPU_THERMTRIP# CPU_PROCHOT# 1.8
RN21 8P4R-330R0402
CPU_TEST19_PLLTEST0 CPU_TEST18_PLLTEST1 CPU_TEST21_SCANEN CPU_TEST26_BURNIN#
RN22 8P4R-10KR0402
CPU_THERMTRIP_D# SMB_THRMCPU_CLK SMB_THRMCPU_DATA CPU_THRM_ALERT- +3VRUN

U2A
VLDT_A3 VLDT_A2 VLDT_A1 VLDT_A0 VLDT_B3 VLDT_B2 VLDT_B1 VLDT_B0
C23 C4.7U6.3X5S0805
L0_CADIN_H15 L0_CADIN_L15 L0_CADIN_H14 L0_CADIN_L14 L0_CADIN_H13 L0_CADIN_L13 L0_CADIN_H12 L0_CADIN_L12 L0_CADIN_H11 L0_CADIN_L11 L0_CADIN_H10 L0_CADIN_L10 L0_CADIN_H9 L0_CADIN_L9 L0_CADIN_H8 L0_CADIN_L8 L0_CADIN_H7 L0_CADIN_L7 L0_CADIN_H6 L0_CADIN_L6 L0_CADIN_H5 L0_CADIN_L5 L0_CADIN_H4 L0_CADIN_L4 L0_CADIN_H3 L0_CADIN_L3 L0_CADIN_H2 L0_CADIN_L2 L0_CADIN_H1 L0_CADIN_L1 L0_CADIN_H0 L0_CADIN_L0
L0_CADOUT_H15 L0_CADOUT_L15 L0_CADOUT_H14 L0_CADOUT_L14 L0_CADOUT_H13 L0_CADOUT_L13 L0_CADOUT_H12 L0_CADOUT_L12 L0_CADOUT_H11 L0_CADOUT_L11 L0_CADOUT_H10 L0_CADOUT_L10 L0_CADOUT_H9 L0_CADOUT_L9 L0_CADOUT_H8 L0_CADOUT_L8 L0_CADOUT_H7 L0_CADOUT_L7 L0_CADOUT_H6 L0_CADOUT_L6 L0_CADOUT_H5 L0_CADOUT_L5 L0_CADOUT_H4 L0_CADOUT_L4 L0_CADOUT_H3 L0_CADOUT_L3 L0_CADOUT_H2 L0_CADOUT_L2 L0_CADOUT_H1 L0_CADOUT_L1 L0_CADOUT_H0 L0_CADOUT_L0
HT_CADOUT15_P HT_CADOUT15_N HT_CADOUT14_P HT_CADOUT14_N HT_CADOUT13_P HT_CADOUT13_N HT_CADOUT12_P HT_CADOUT12_N HT_CADOUT11_P HT_CADOUT11_N HT_CADOUT10_P HT_CADOUT10_N HT_CADOUT9_P HT_CADOUT9_N HT_CADOUT8_P HT_CADOUT8_N HT_CADOUT7_P HT_CADOUT7_N HT_CADOUT6_P HT_CADOUT6_N HT_CADOUT5_P HT_CADOUT5_N HT_CADOUT4_P HT_CADOUT4_N HT_CADOUT3_P HT_CADOUT3_N HT_CADOUT2_P HT_CADOUT2_N HT_CADOUT1_P HT_CADOUT1_N HT_CADOUT0_P HT_CADOUT0_N
HT_CLKIN1_P HT_CLKIN1_N HT_CLKIN0_P HT_CLKIN0_N
L0_CTLIN_H1 L0_CTLIN_L1 L0_CTLIN_H0 L0_CTLIN_L0
L0_CTLOUT_H1 L0_CTLOUT_L1 L0_CTLOUT_H0 L0_CTLOUT_L0
HT_CLKOUT1_P HT_CLKOUT1_N HT_CLKOUT0_P HT_CLKOUT0_N
R190 51R0402 R189 51R0402 HT_CTLIN1_P HT_CTLIN1_N
HT_CTLOUT1_P HT_CTLOUT1_N
HT_CTLIN0_P HT_CTLIN0_N HT_CTLOUT0_P HT_CTLOUT0_N
TP13 TP12
Athlon 64 S1 Processor Socket

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

SB_CPUPWRGD R369 0R0402 CPU_ALL_PWROK
LDT_STOP# R370 0R0402 CPU_LDTSTOP#
LDT_RST# R371 0R0402 CPU_HT_RESET#
RN42 8P4R-10KR0402

+1.8VRUN +3VSUS
RN18 X_8P4R-1KR0402
RN19 X_8P4R-330R0402
17 SB_CPUPWRGD
CPU_SPI#_L CPU_ALL_PWROK CPU_LDTSTOP# CPU_HT_RESET#
13,17 LDT_STOP#
17 LDT_RST#
34,37 VDD_PG
U18A X_LCX07MTCTSSOP14
U18B X_LCX07MTCTSSOP14
U18C X_LCX07MTCTSSOP14
U18D X_LCX07MTCTSSOP14
U18E X_LCX07MTCTSSOP14
U18F X_LCX07MTCTSSOP14

+3VALW +3VSUS
Cap close to thermal sensor
Close to CPU socket
R367 X_0R0402
R327 0R0402
CPU_TEST4_THERMDA
C277 C2200P50X0402
CPU_TEST5_THERMDC
U20
VDD D+ D- T_CRIT_A SMBCLK SMBData ALERT GND
LM86CIMMXNOPB_MSOP8-RH
SMB_THRMCPU_CLK SMB_THRMCPU_DATA
SMB_THRMCPU_CLK 30 SMB_THRMCPU_DATA 30 CPU_THRM_ALERT- 30
C278 C0.1U16V0402
R193 X_10KR0402
R368 X_0R0402
34 T_CRIT_CPU#

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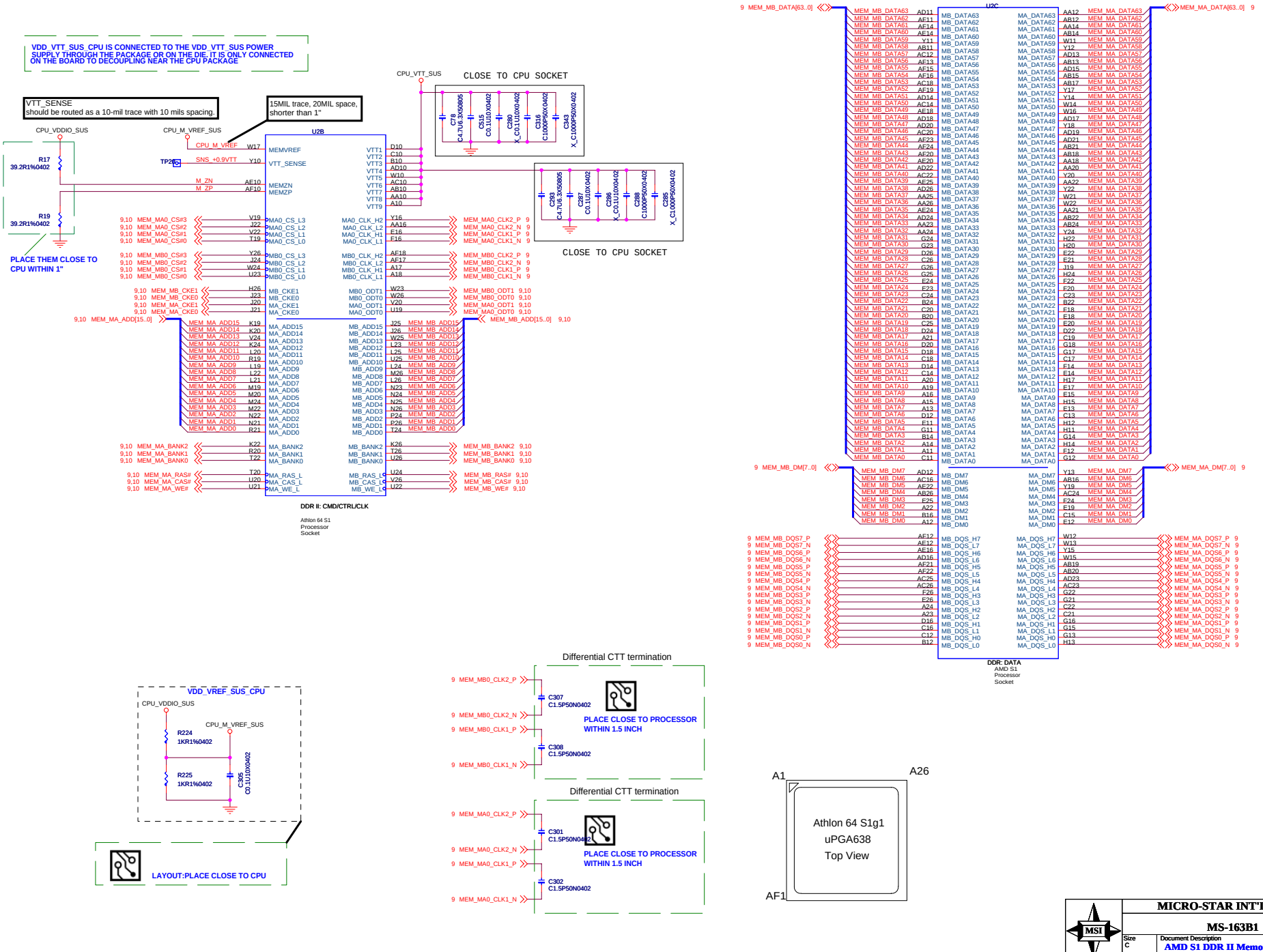
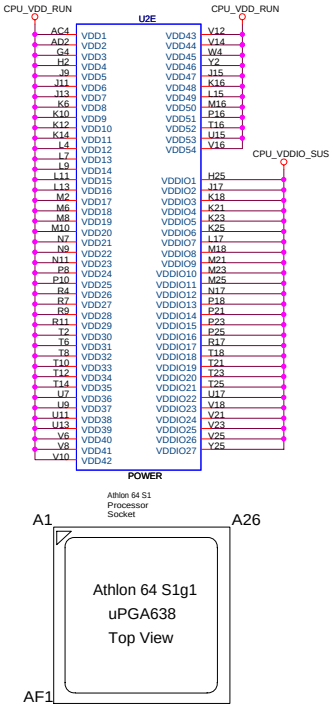
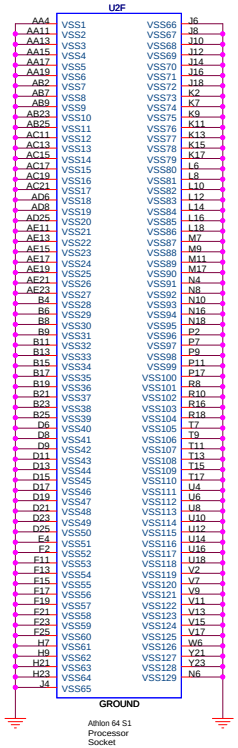
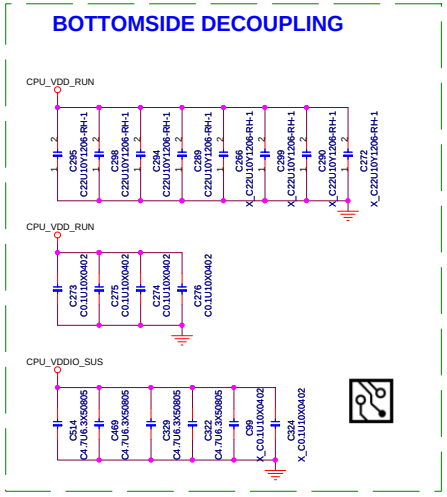
Processor DDR2 Memory Interface



MICRO-STAR INT'L CO.,LTD	
MS-163B1	
Size: C	Document Description: AMD S1 DDR II Memory I/F
Rev: 0A	
Date: Monday, April 23, 2007	Sheet 7 of 40

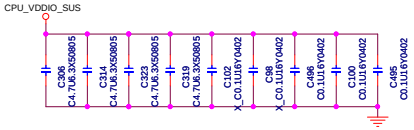






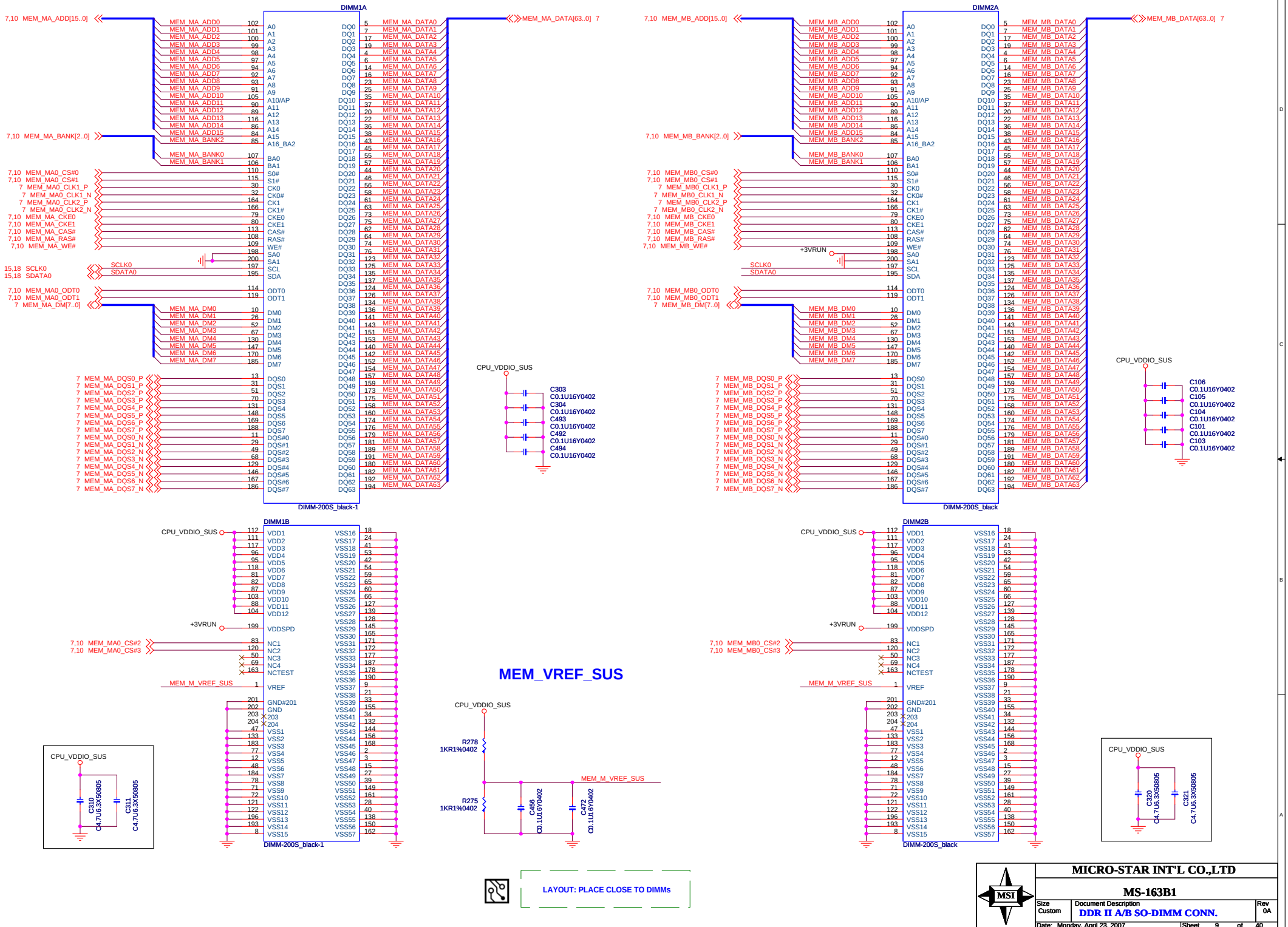
DECOUPLING BETWEEN PROCESSOR AND DIMMs

PLACE CLOSE TO PROCESSOR AS POSSIBLE



PROCESSOR POWER AND GROUND

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-163B1	
Size: C	Document Description: AMD S1 Power & GND	Rev: 0A
Date: Monday, April 23, 2007	Sheet 8 of 40	


DIMM1A
DIMM-200S_black-1
DIMM2A
DIMM-200S_black
DIMM1B
DIMM-200S_black-1
DIMM2B
DIMM-200S_black
MEM_VREF_SUS
LAYOUT: PLACE CLOSE TO DIMMs
MICRO-STAR INT'L CO.,LTD
MS-163B1
DDR II A/B SO-DIMM CONN.
Size Custom
Rev 0A
Date: Monday, April 23, 2007
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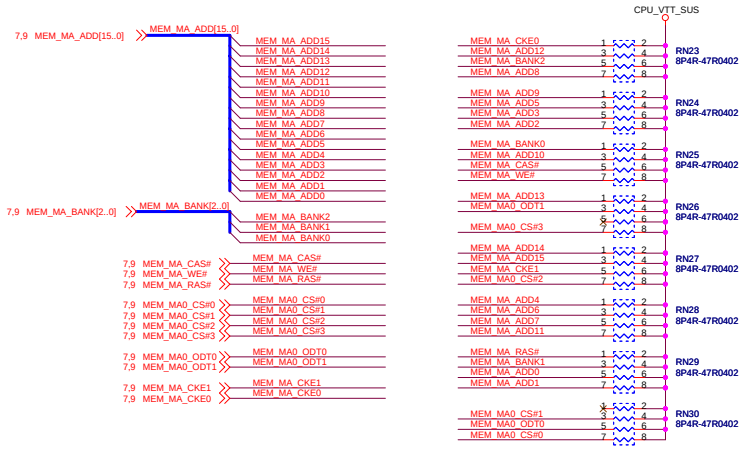

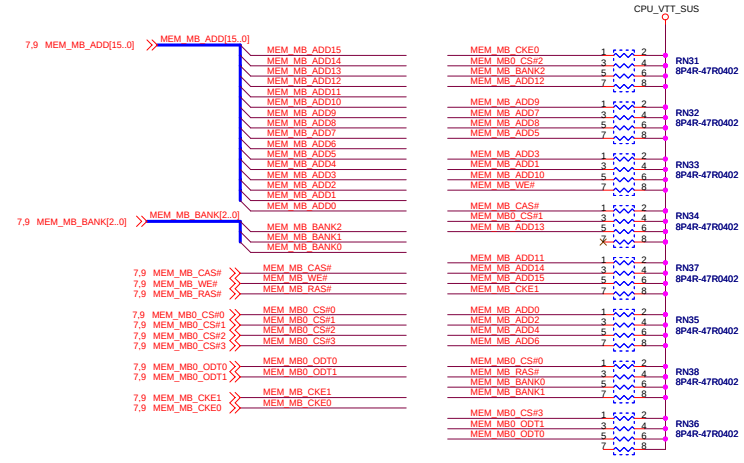

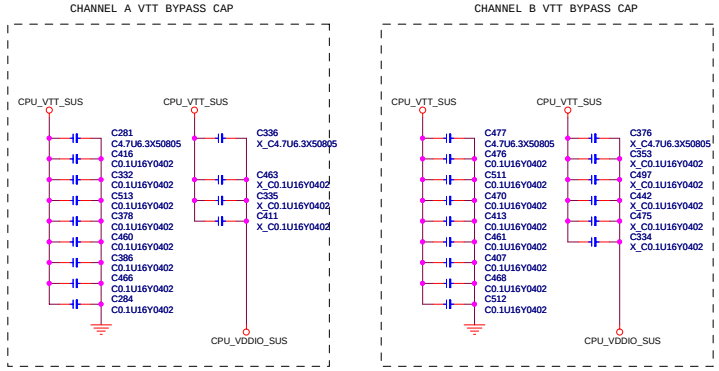

MICRO-STAR INT'L CO.,LTD

MS-163B1

Size	Document Description	Rev
C	DDR II A/B Terminations	0A

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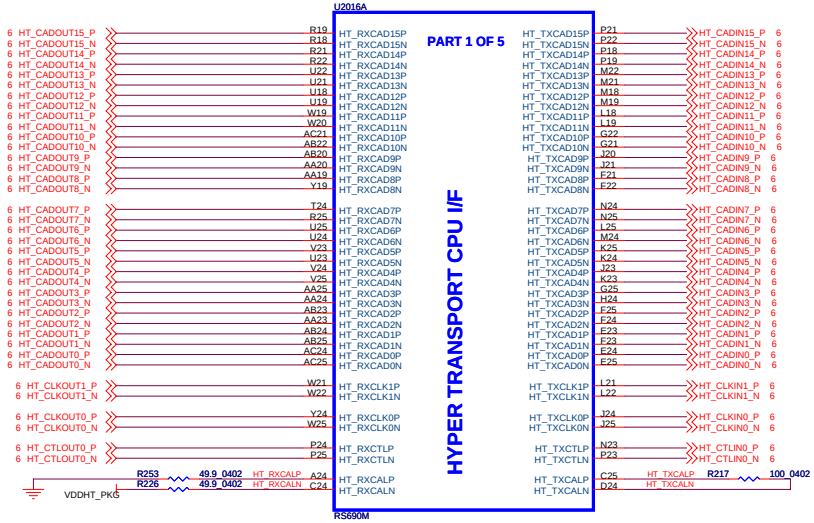

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	RS690M HT LINK I/F		
Size C	Document Number MS-163B1		Rev 0A
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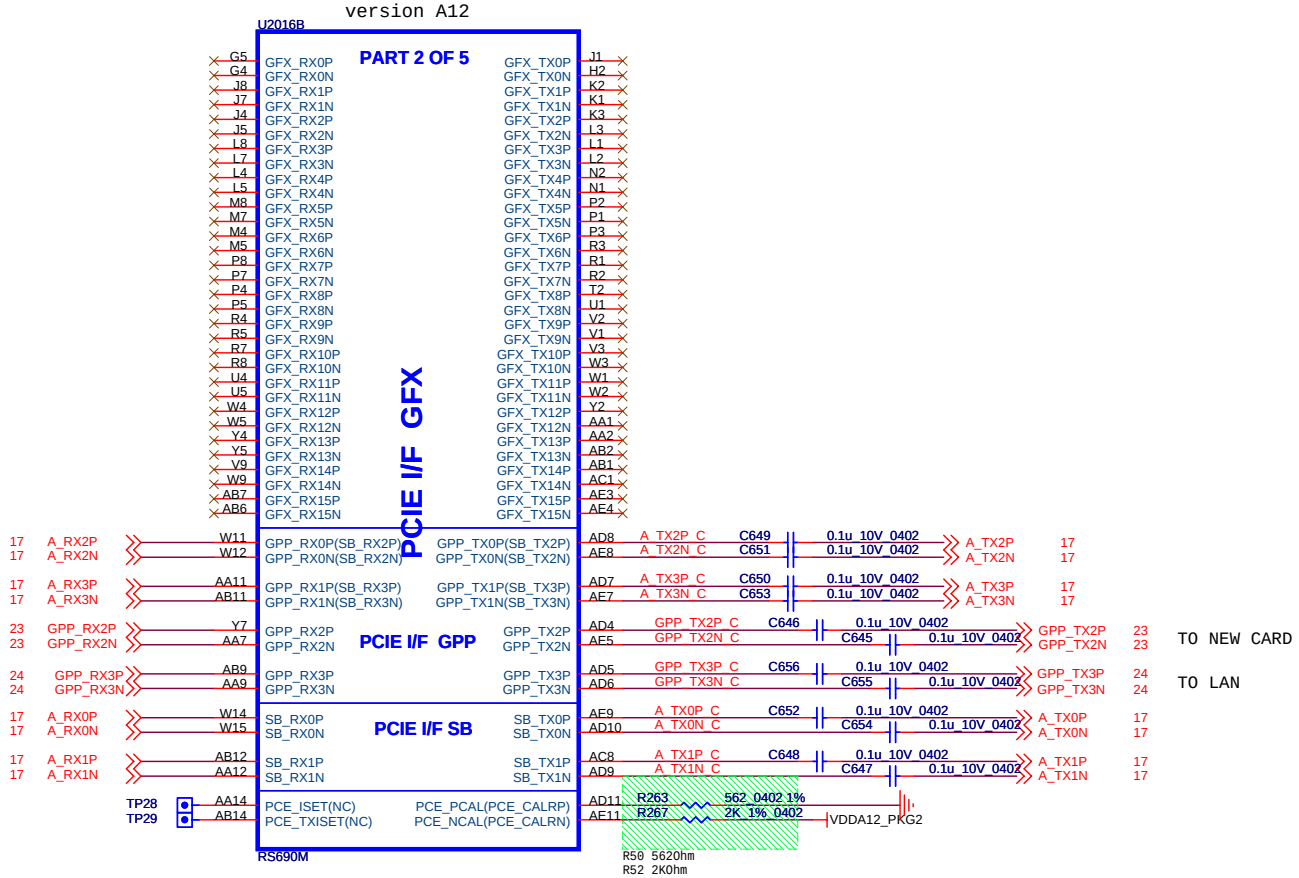
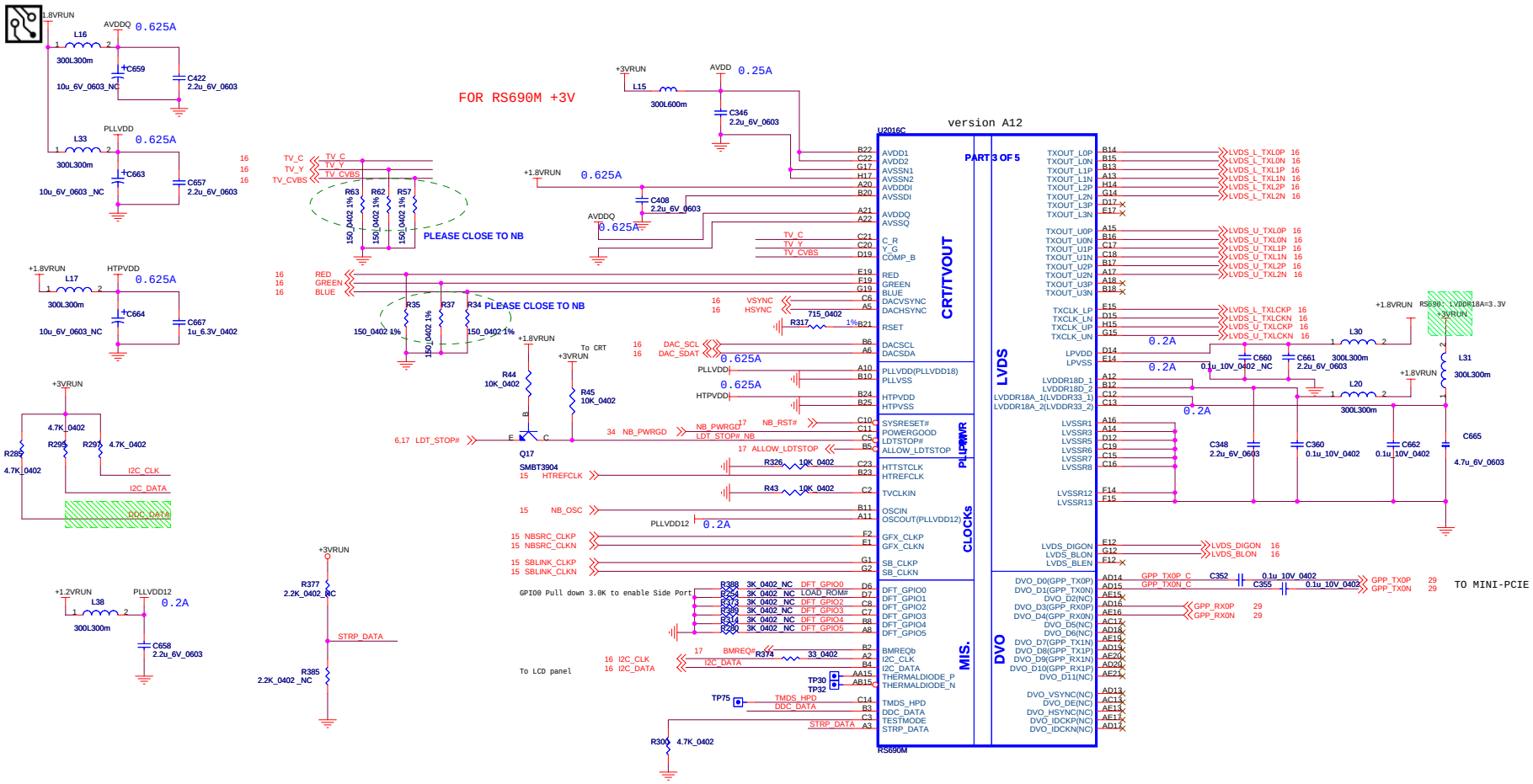
version A12



MICRO-STAR INT'L CO.,LTD.			
Title: RS690T PCI-E LINK&HDMI I/F			
Size: B	Document Number: MS-163B1		Rev: 0A
Date: Monday, April 23, 2007	Sheet 12 of 40		



	RS485/RS690	RS690 only (NC for RS485)		
	DFT_GPIO1	DFT_GPIO0	DFT_GPIO[4:2]	DFT_GPIO5
PULL HIGH (internally pulled high)	Bypass the loading of EEPROM straps and use Hardware default values DEFAULT	Memory side port not available DEFAULT	These pin straps are used to configure PCI-E GPP mode: 111: register defined (register default to Config E) DEFAULT 110: 4-0-0-0-0 Config A 101: 4-4 Config B 100: 4-2-2 Config C 011: 4-2-1-1 Config D 010: 4-1-1-1-1 Config E others: register defined (register default to Config E)	Enable debug bus via the memory IO pads, if available in the package use default values DEFAULT
PULL LOW	I2C Master can load strap values from EEPROM if connected, or use default values if not connected	Memory side port available		use the memory data bus to output the debug bus

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	RS690T SYSTEM I/F&CLK	
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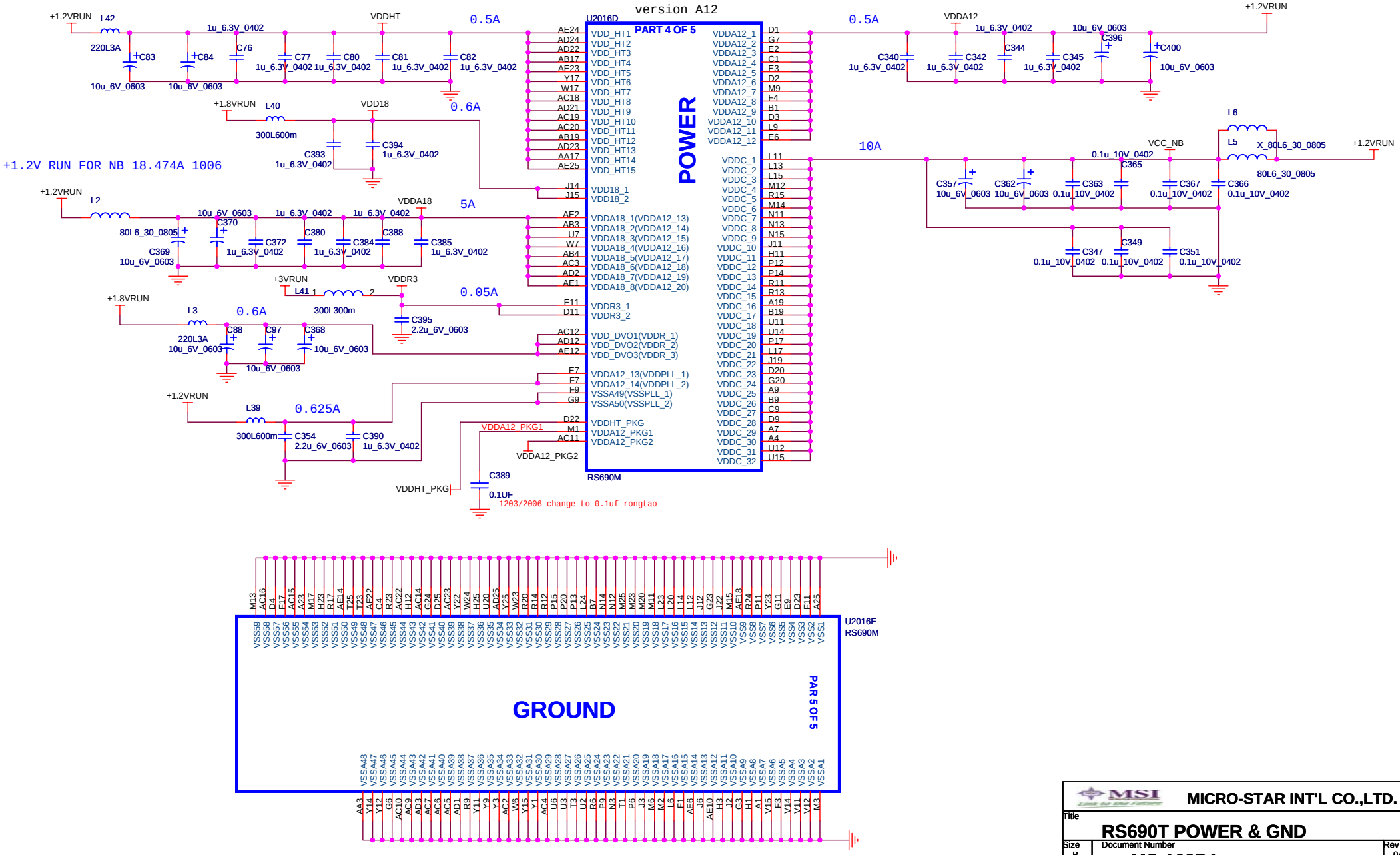

MICRO-STAR INT'L CO.,LTD.			
Title: RS690T POWER & GND			
Size: B	Document Number: MS-163B1		Rev: 0A
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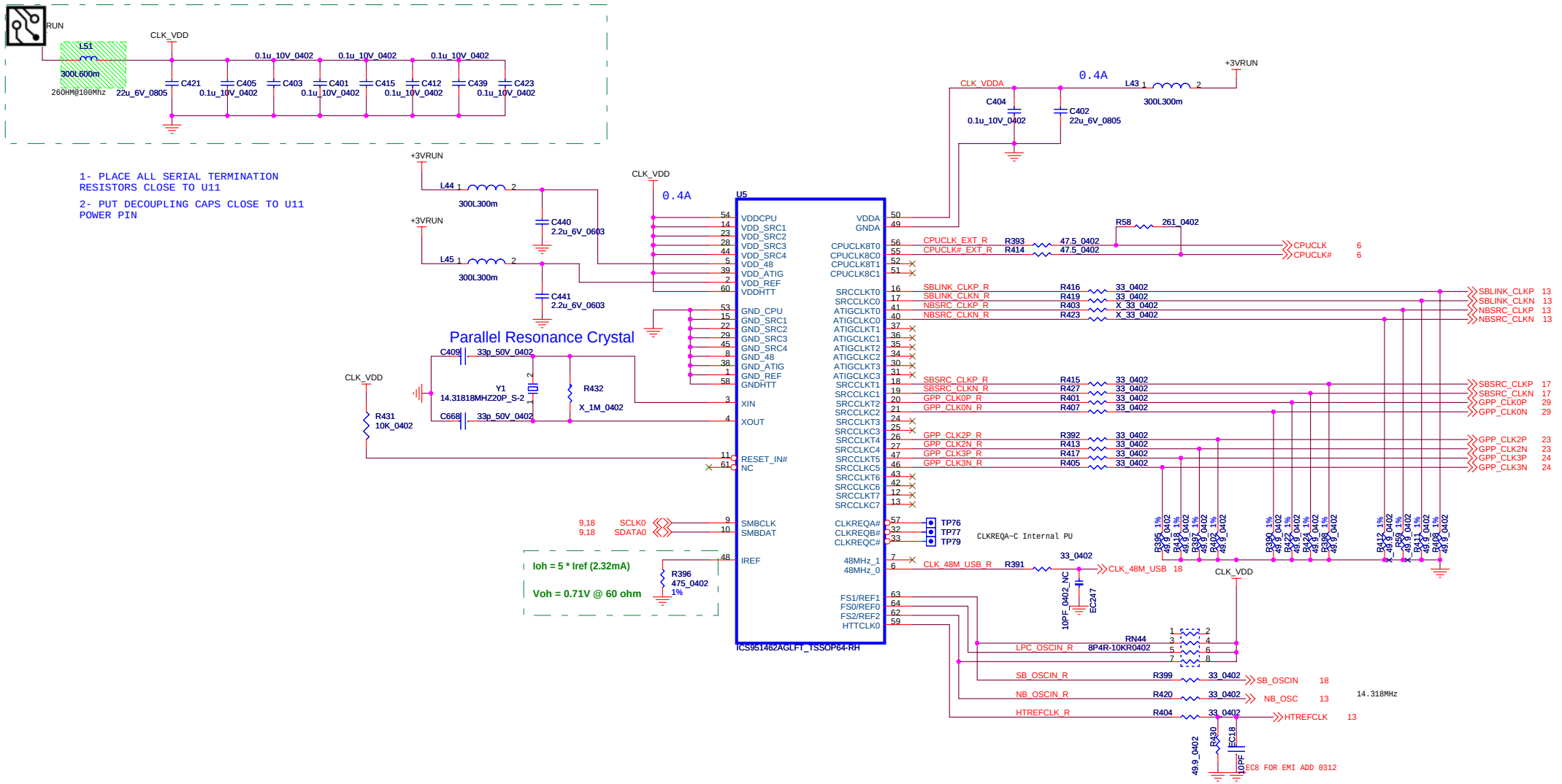
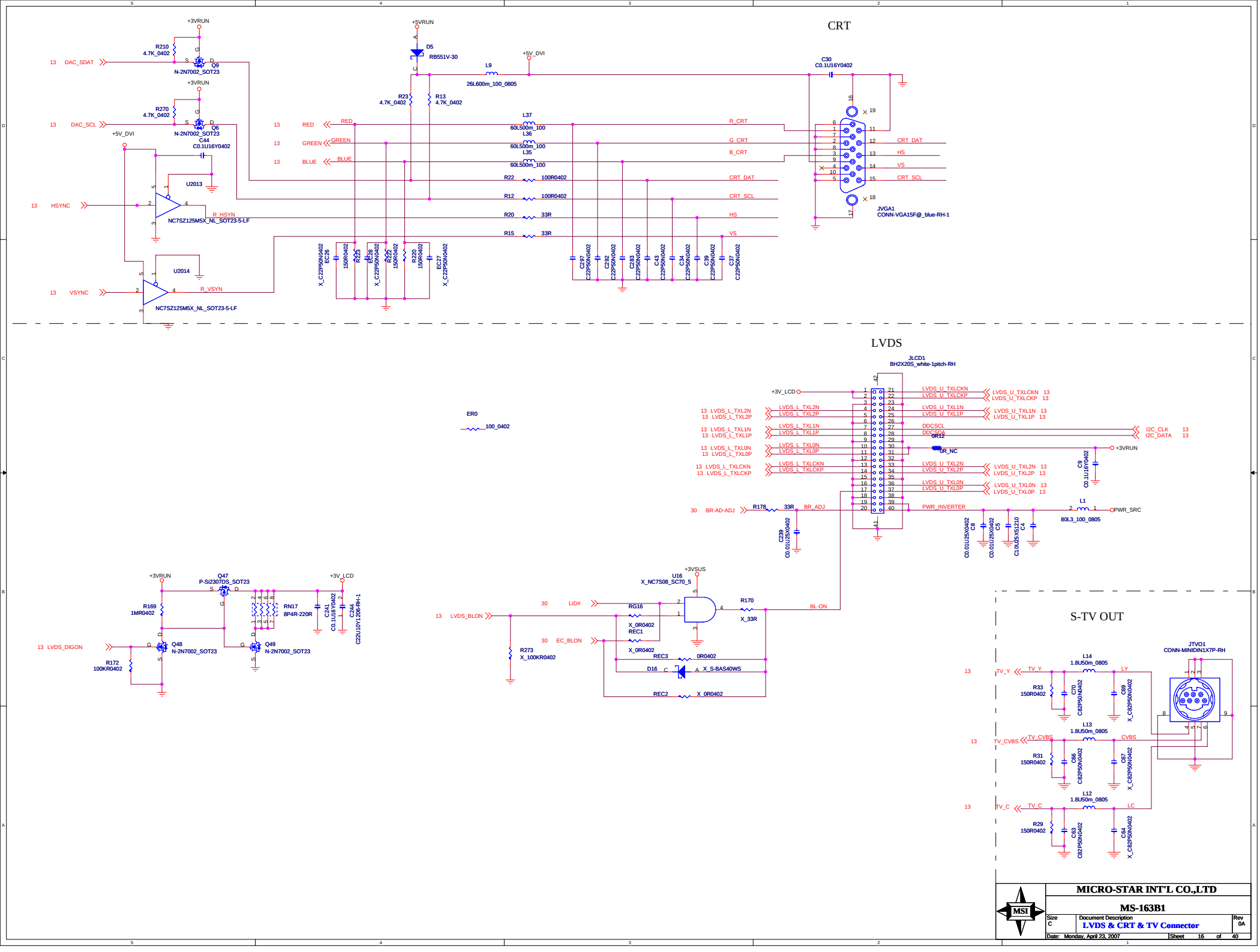
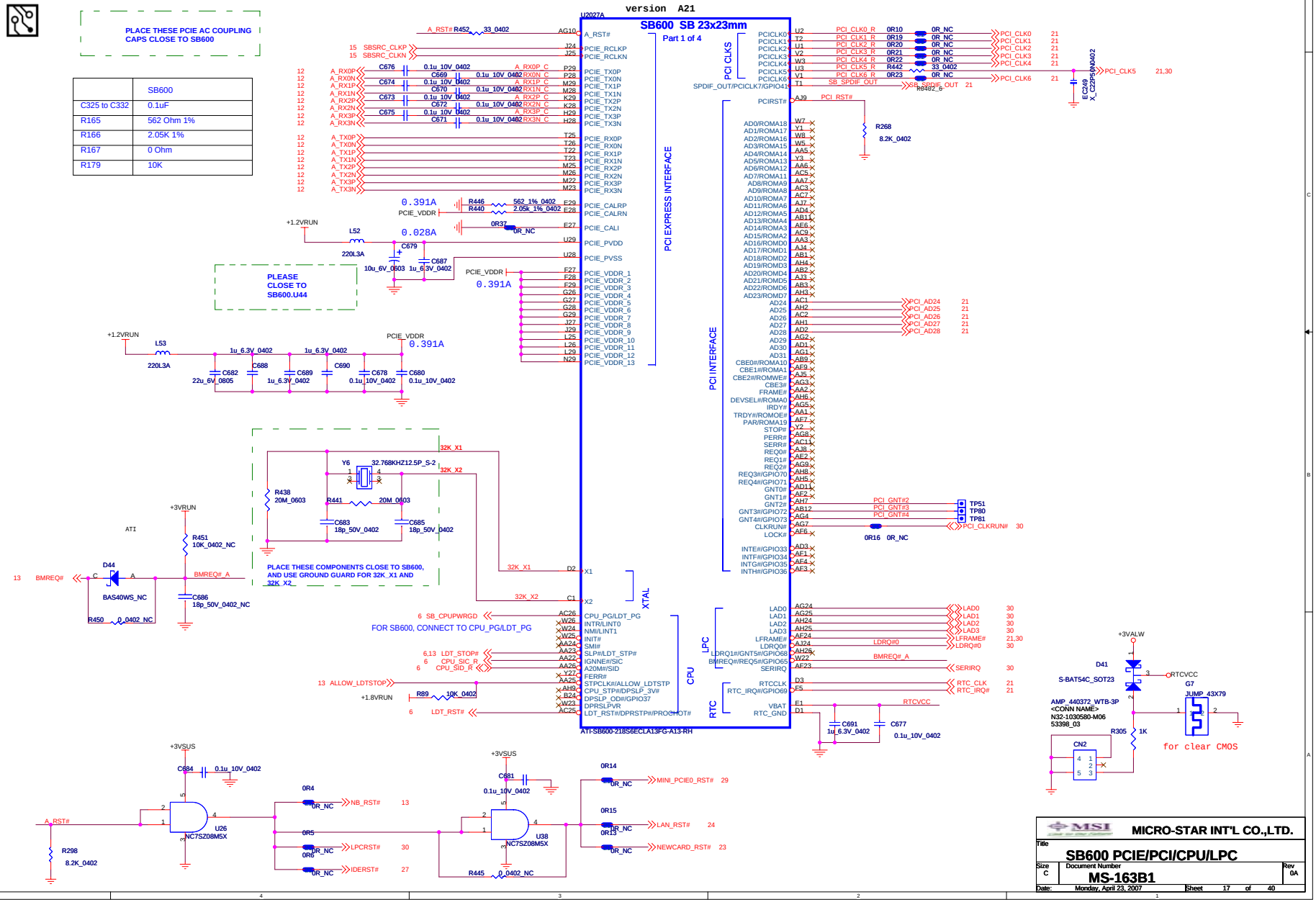
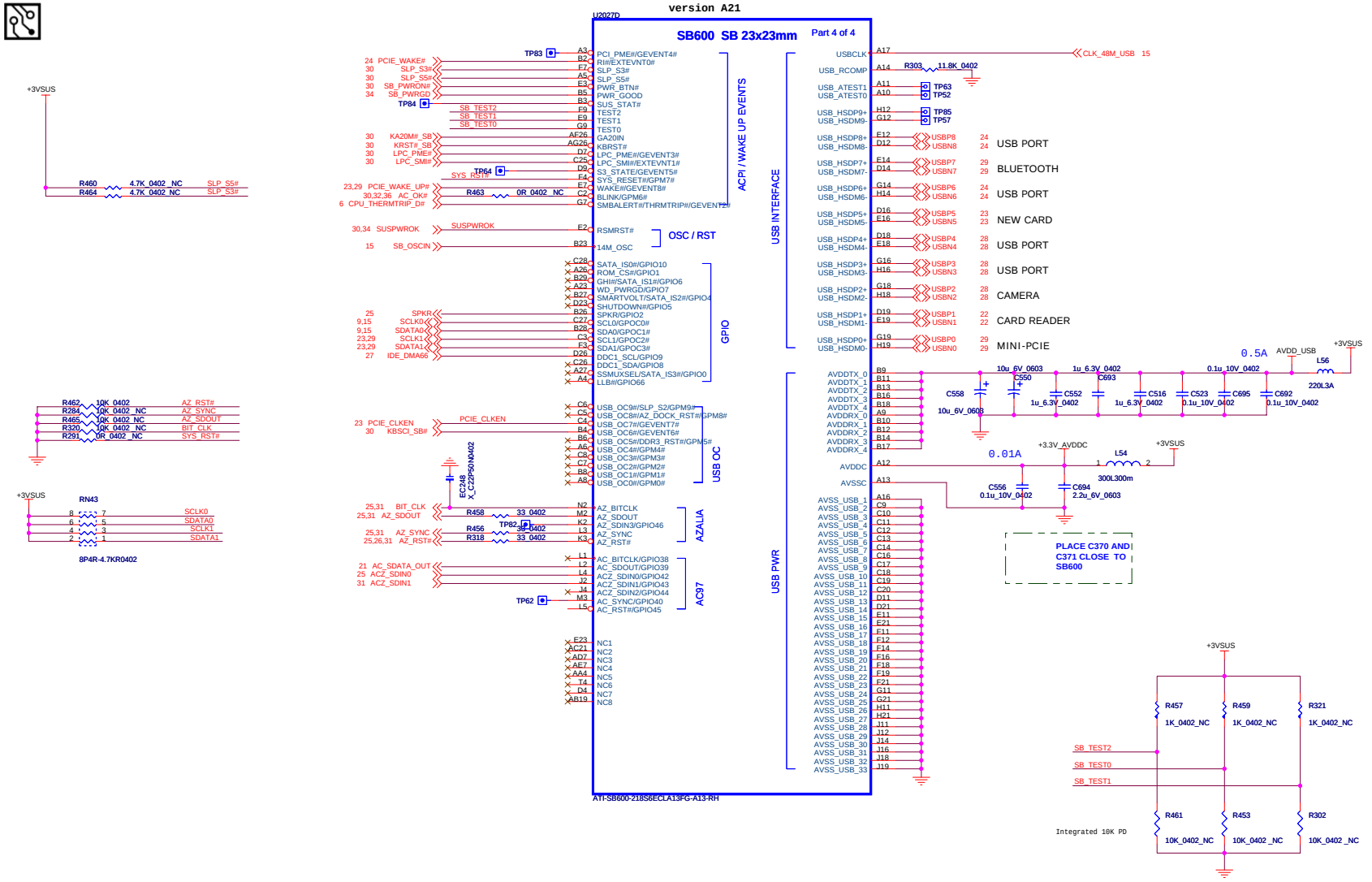


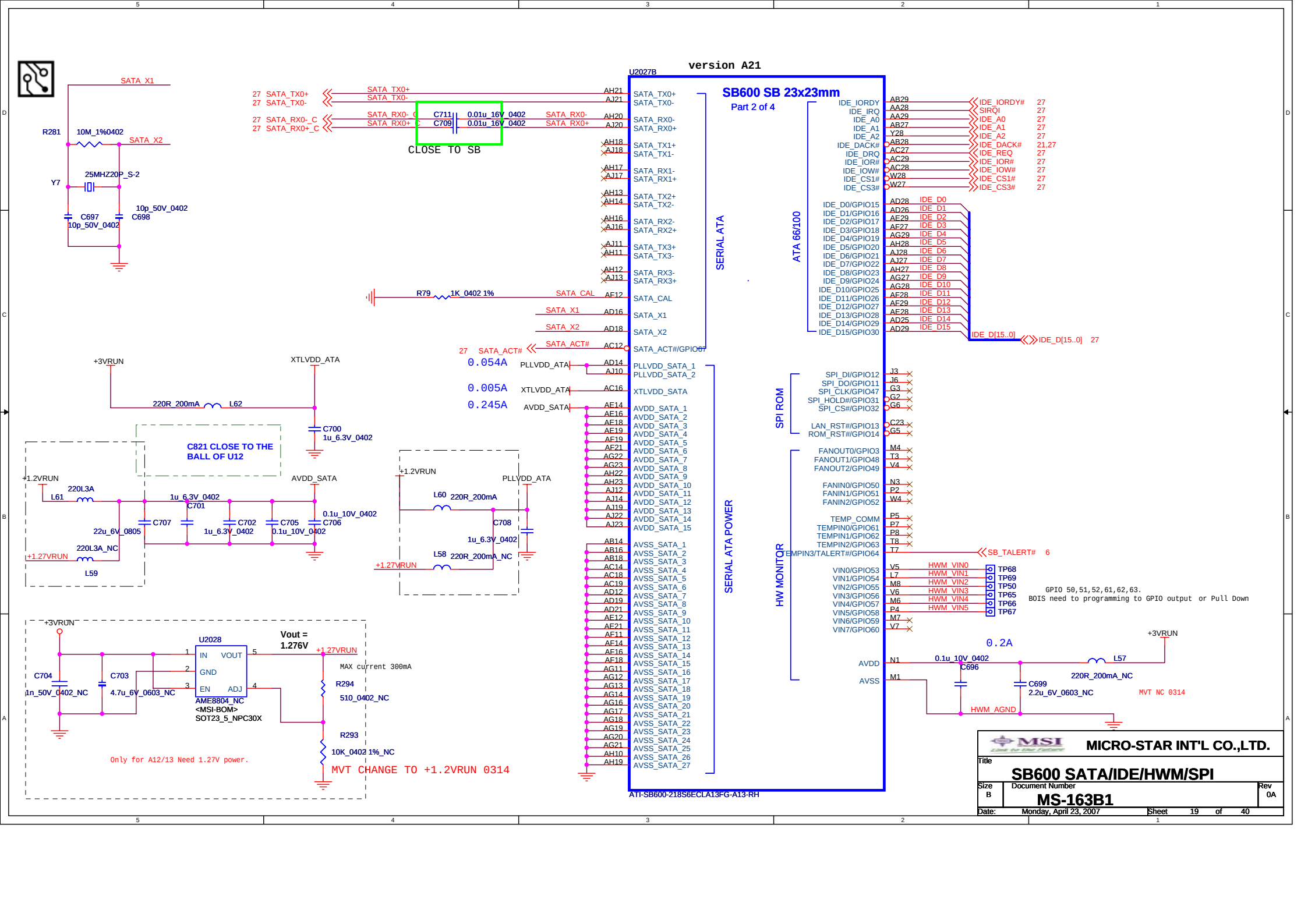
MSI	MICRO-STAR INT'L CO.,LTD.	
Title	CLOCK GENERATOR	
Size: Custom	Document Number: MS-163B1	Rev: 0A
Date: Monday, April 23, 2007	Sheet 15 of 40	


CRT
LVDS
S-TV OUT
+3VRUN
+5VRUN
+5V_DVI
+3V_LCD
+3VSUS
R210 4.7K_0402
R270 4.7K_0402
Q9 N-2N7002_SOT23
Q6 N-2N7002_SOT23
D5 RB551V-30
L9 26L600m_100_0805
C30 C0.1U16Y0402
C44 C0.1U16Y0402
R23 4.7K_0402
R13 4.7K_0402
DAC_SDAT
DAC_SCL
HSYNC
VSYNC
U2013 NC7SZ125M5X_NL_SOT23-5-LF
U2014 NC7SZ125M5X_NL_SOT23-5-LF
R_HSYN
R_VSYN
RED
GREEN
BLUE
L37 60L500m_100
L36 60L500m_100
L35 60L500m_100
R22 100R0402
R12 100R0402
R20 33R
R15 33R
R_CRT
G_CRT
B_CRT
CRT_DAT
CRT_SCL
HS
VS
JVGA1 CONN-VGA15F@_blue-RH-1
JLCD1 BH2X20S_white-1pitch-RH
ER0 100_0402
0R12 0R_NC
R178 33R
BR_ADJ
BR-AD-ADJ
PWR_INVERTER
L1 80L3_100_0805
PWR_SRC
I2C_CLK
I2C_DATA
LVDS_L_TXL2N
LVDS_L_TXL2P
LVDS_L_TXL1N
LVDS_L_TXL1P
LVDS_L_TXL0N
LVDS_L_TXL0P
LVDS_L_TXLCKN
LVDS_L_TXLCKP
LVDS_U_TXL2N
LVDS_U_TXL2P
LVDS_U_TXL1N
LVDS_U_TXL1P
LVDS_U_TXL0N
LVDS_U_TXL0P
LVDS_U_TXLCKN
LVDS_U_TXLCKP
DDCSCL
DDCSDA
Q47 P-Si2307DS_SOT23
Q48 N-2N7002_SOT23
Q49 N-2N7002_SOT23
R169 1MR0402
R172 100KR0402
RN17 8P4R-220R
C241 C0.1U16Y0402
C244 C22U10Y1206-RH-1
LVDS_DIGON
LVDS_BLON
U16 X_NC7S08_SC70_5
LID#
EC_BLON
RG16 X_0R0402
REC1 X_0R0402
REC3 0R0402
REC2 X_0R0402
D16 X_S-BAS40WS
R170 X_33R
R273 X_100KR0402
BL-ON
JTVO1 CONN-MINIDIN1X7P-RH
L14 1.8U50m_0805
L13 1.8U50m_0805
L12 1.8U50m_0805
TV_Y
TV_CVBS
TV_C
LY
CVBS
LC
R33 150R0402
R31 150R0402
R29 150R0402
MICRO-STAR INT'L CO.,LTD
MS-163B1
Size C
Document Description
LVDS & CRT & TV Connector
Rev 0A
Date: Monday, April 23, 2007
Sheet 16 of 40

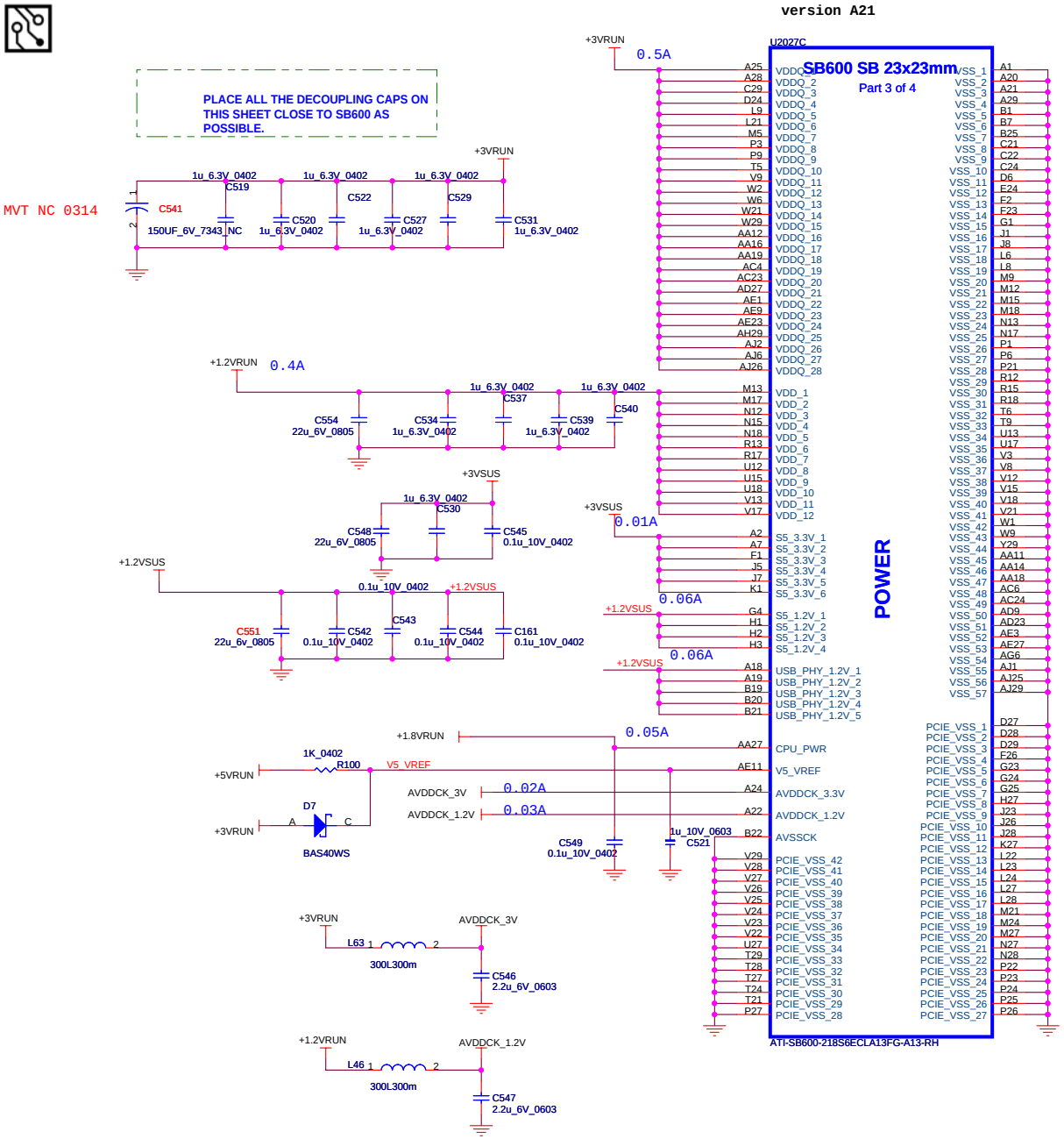

version A21
U2027A
SB600 SB 23x23mm
Part 1 of 4
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB600
SB600
C325 to C332 0.1uF
R165 562 Ohm 1%
R166 2.05K 1%
R167 0 Ohm
R179 10K
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
XTAL
LPC
CPU
RTC
PLEASE CLOSE TO SB600.U44
PLACE THESE COMPONENTS CLOSE TO SB600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
FOR SB600, CONNECT TO CPU_PG/LDT_PG
ATI-SB600-218S6ECLA13FG-A13-RH
for clear CMOS
MICRO-STAR INT'L CO.,LTD.
SB600 PCIE/PCI/CPU/LPC
MS-163B1
Monday, April 23, 2007
Sheet 17 of 40



MSI	MICRO-STAR INT'L CO.,LTD.
Title	SB600 ACPI/GPIO/USB/AUDIO
Size C	Document Number MS-163B1 Rev 0A
Date: Monday, April 23, 2007	Sheet 18 of 40


version A21
U2027B
SB600 SB 23x23mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SATA_X1
R281 10M_1%0402
SATA_X2
Y7 25MHZ20P_S-2
C697 10p_50V_0402
C698 10p_50V_0402
CLOSE TO SB
C711 0.01u_16V_0402
C709 0.01u_16V_0402
R79 1K_0402 1%
SATA_CAL
SATA_ACT#
0.054A
0.005A
0.245A
+3VRUN
XTLVDD_ATA
220R_200mA
L62
C700 1u_6.3V_0402
C821 CLOSE TO THE BALL OF U12
+1.2VRUN
AVDD_SATA
L61 220L3A
C701 1u_6.3V_0402
C707 22u_6V_0805
C702 1u_6.3V_0402
C705 0.1u_10V_0402
C706 0.1u_10V_0402
+1.27VRUN
L59 220L3A_NC
PLLVDD_ATA
L60 220R_200mA
C708 1u_6.3V_0402
L58 220R_200mA_NC
U2028
Vout = 1.276V
AME8804_NC
<MSI-BOM>
SOT23_5_NPC30X
C704 1n_50V_0402_NC
C703 4.7u_6V_0603_NC
R294 510_0402_NC
R293 10K_0402 1%_NC
MAX current 300mA
Only for A12/13 Need 1.27V power.
MVT CHANGE TO +1.2VRUN 0314
ATI-SB600-218S6ECLA13FG-A13-RH
GPIO 50,51,52,61,62,63.
BOIS need to programming to GPIO output or Pull Down
0.2A
AVDD
AVSS
C696 0.1u_10V_0402
C699 2.2u_6V_0603_NC
L57 220R_200mA_NC
HWM_AGND
MVT NC 0314
MICRO-STAR INT'L CO.,LTD.
Title
SB600 SATA/IDE/HWM/SPI
Size B
Document Number MS-163B1
Rev 0A
Date: Monday, April 23, 2007
Sheet 19 of 40

version A21

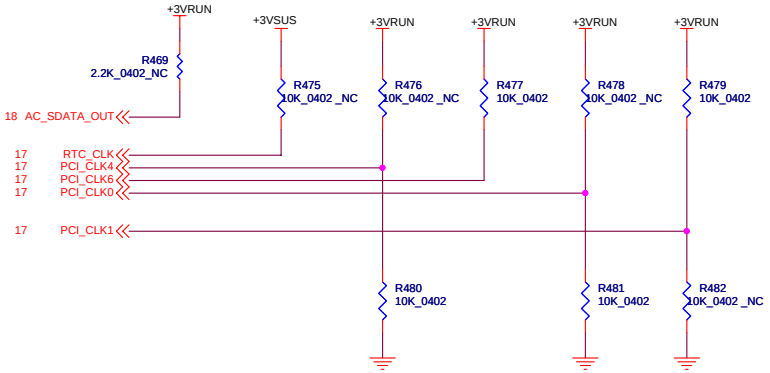


Title	SB600 POWER & GND
Size	Custom
Document Number	MS-163B1
Rev	0A
Date:	Monday, April 23, 2007
Sheet	20 of 40

MICRO-STAR INT'L CO.,LTD.

REQUIRED STRAPS

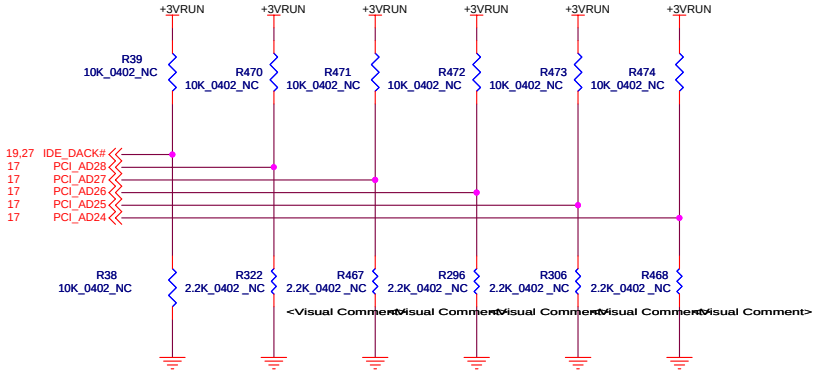
NPTE: FOR SB460, EXTERNAL PU/PD ARE REQUIRED



	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	SB600 PCI_CLK0	SB600 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

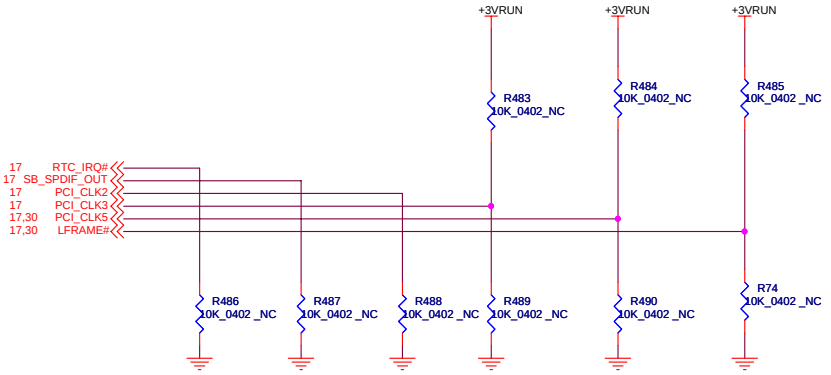
DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[31:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS

SPDIF_OUT Integrated 10K
PM2_Rg EAh. Default: PU/PD not enable
BIOS must confirm with AMI/ATI.



	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

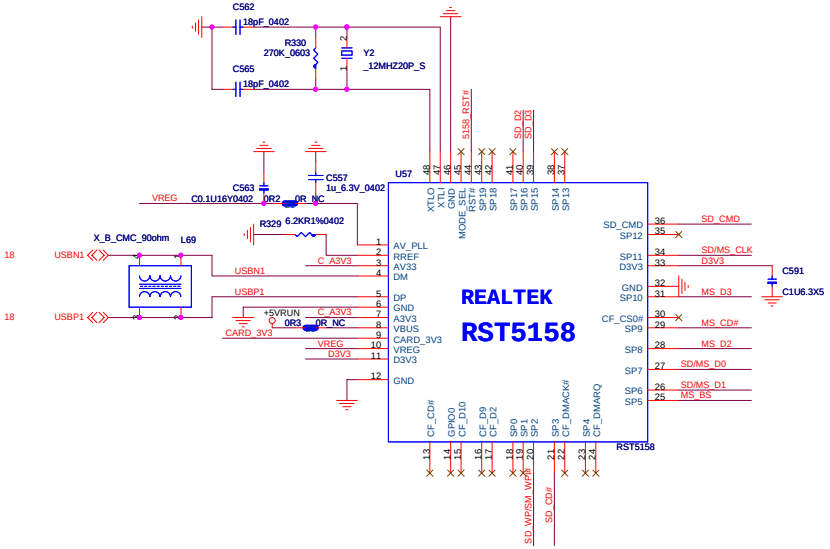
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

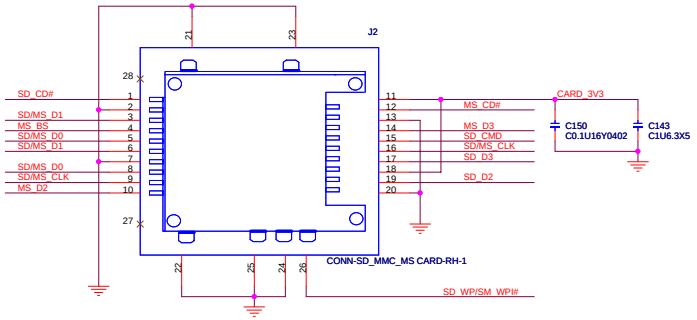
MICRO-STAR INT'L CO.,LTD.

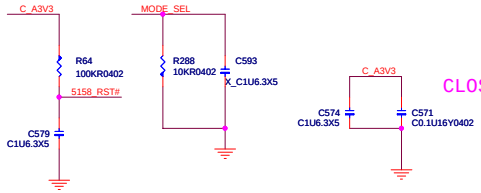
Title: SB600 STRAPS

Size: Custom | Document Number: MS-163B1 | Rev: 0A

Date: Monday, April 23, 2007 | Sheet 21 of 40







CLOSE TO RST5158

J2 : SD/MS DEVIC

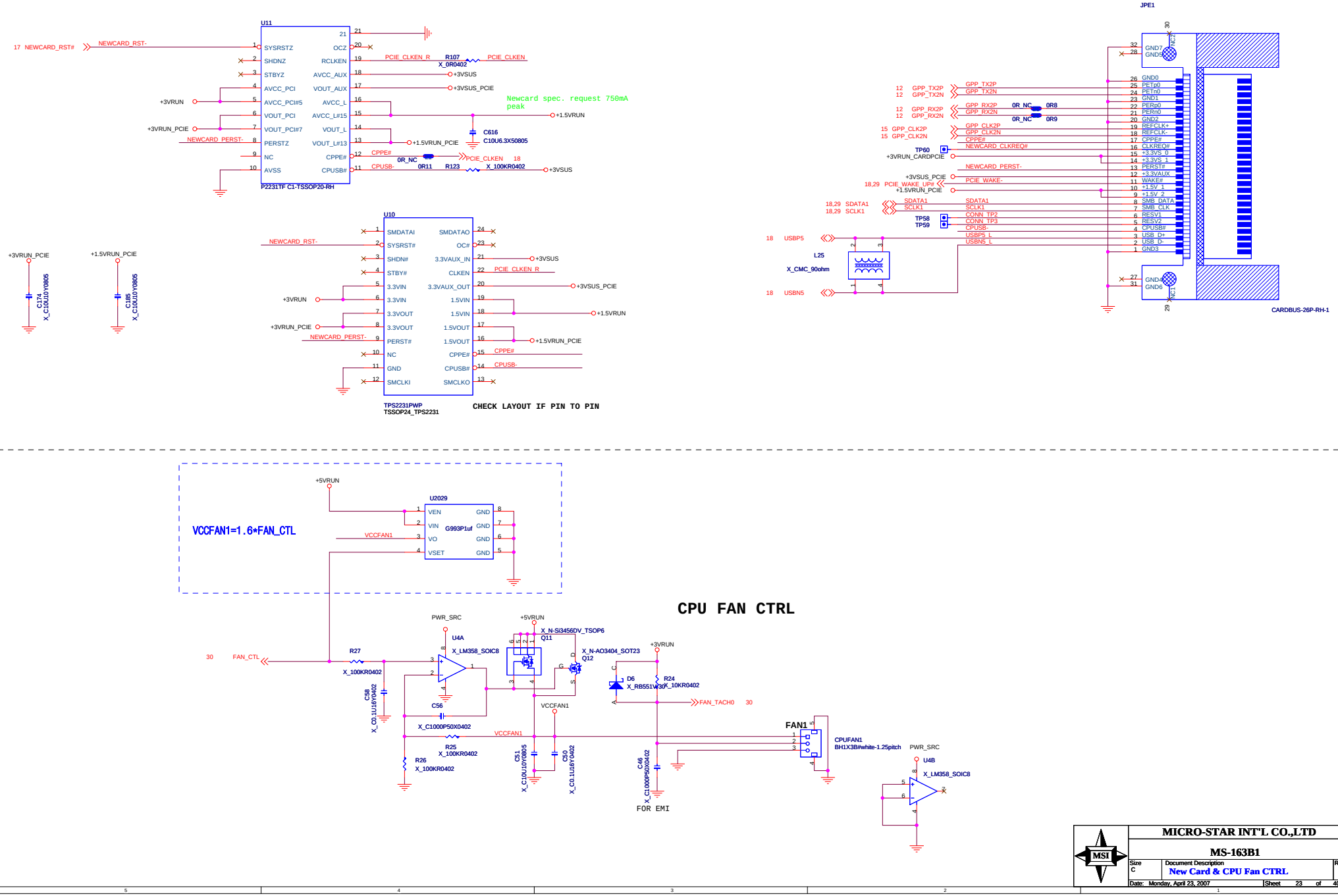
Pin	Description	Pin	Description
1	**Card Detect SW**	2	**MS VSS**
3	**SD Data1**	4	**MS BS**
5	**SD Data0**	6	**MS Data1**
7	**SD VSS**	8	**MS Data0**
9	**SD CLK**	10	**MS Data2**
11	**SD VDD**	12	**MS INS**
13	**SD VSS**	14	**MS Data3**
15	**SD CMD**	16	**MS CLK**
17	**SD Data3**	18	**MS VDD**
19	**SD Data2**	20	**MS VSS**
		26	**SD_WP**

MICRO-STAR INT'L CO.,LTD

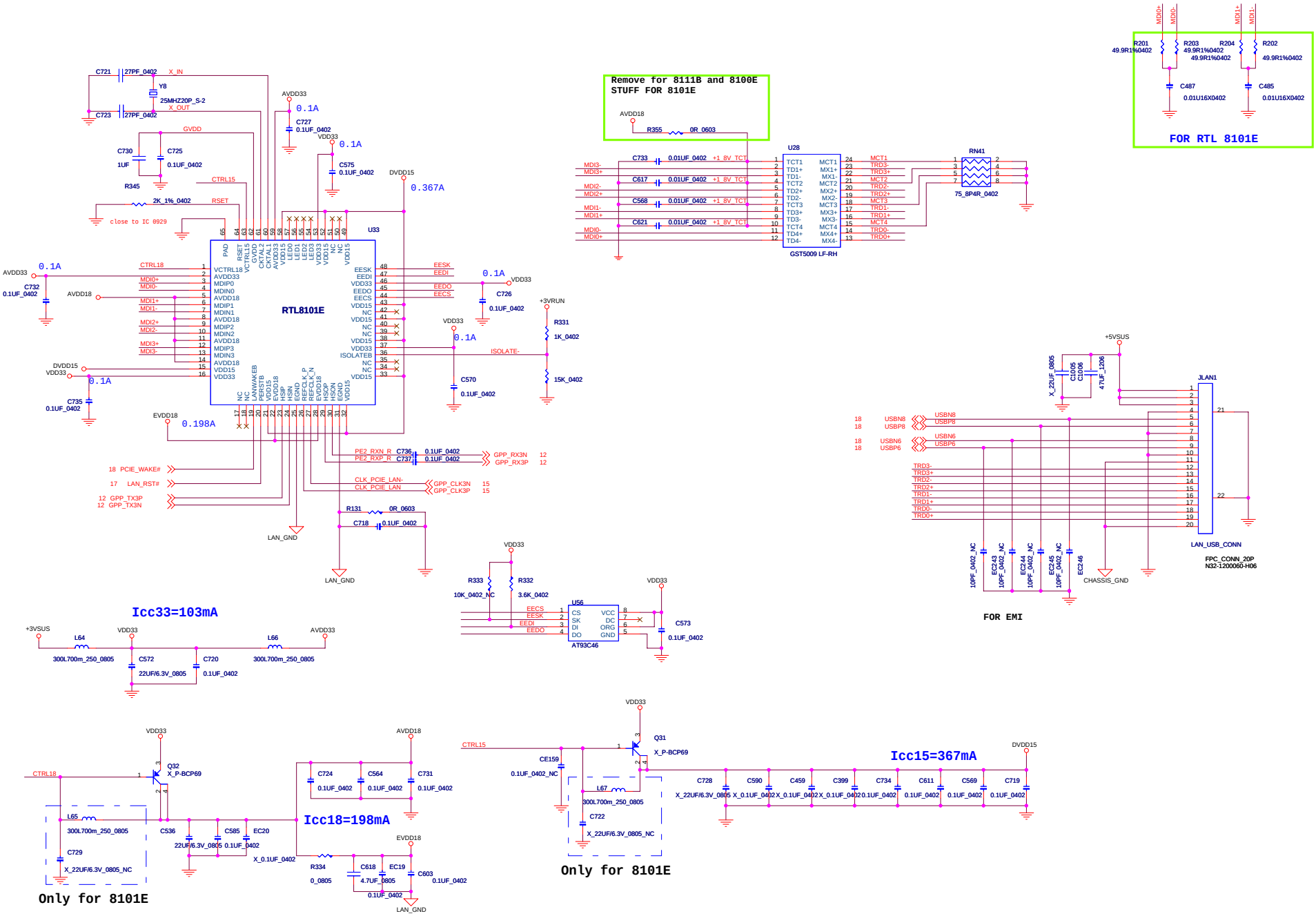
MS-163B1

Size	Document Description	Rev
C	Card Reader (RTS5158)	0A

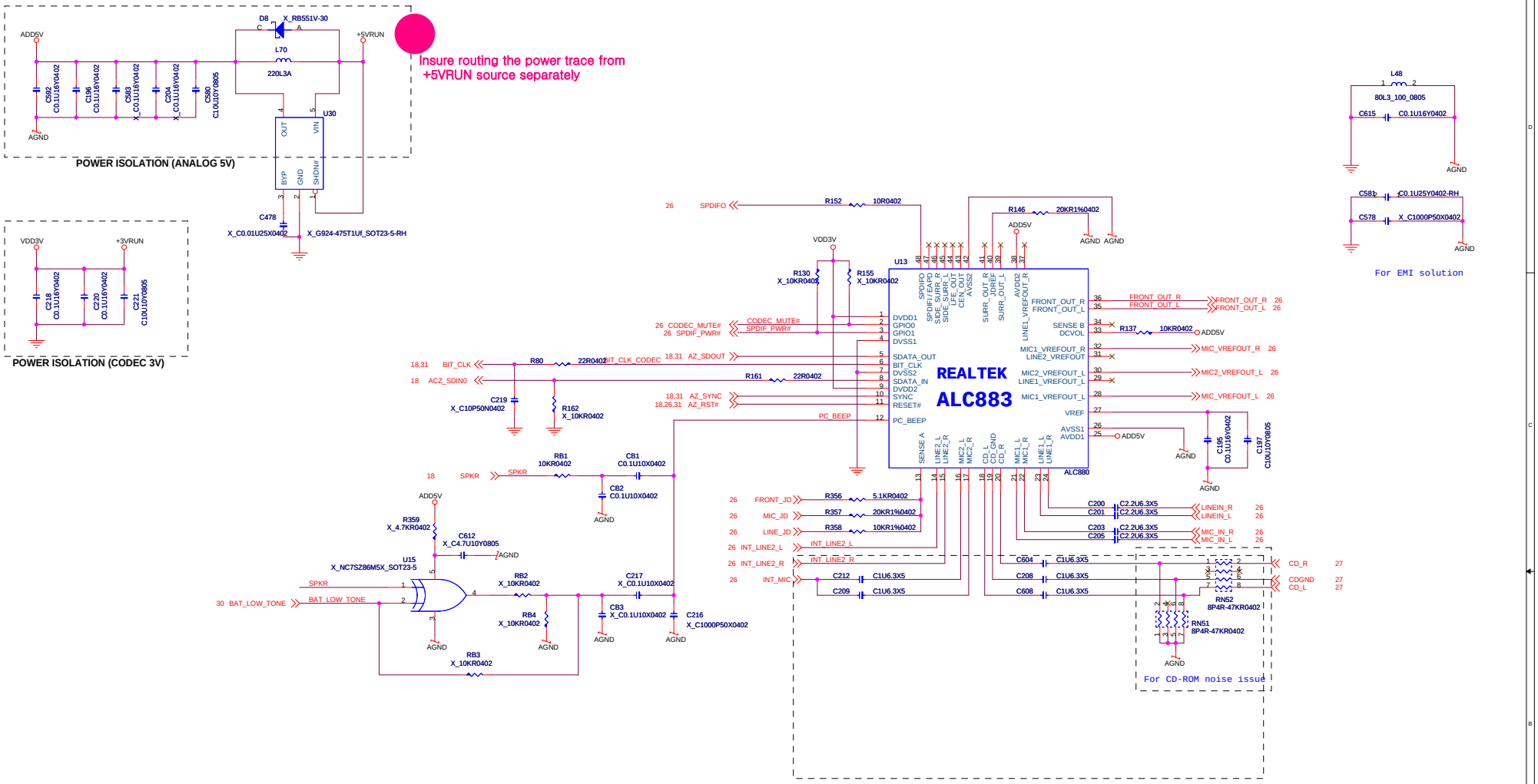
Date: Monday, April 23, 2007 | Sheet 22 of 40



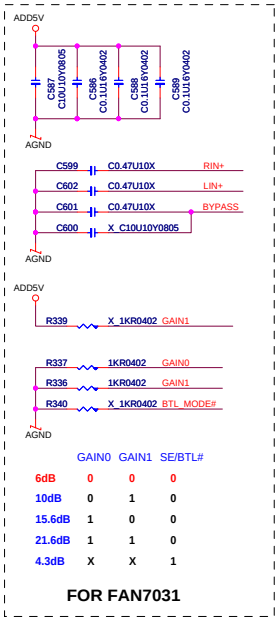
MICRO-STAR INT'L CO.,LTD			
MS-163B1			
Size: C	Document Description: New Card & CPU Fan CTRL		Rev: 0A
Date: Monday, April 23, 2007		Sheet 23 of 40	

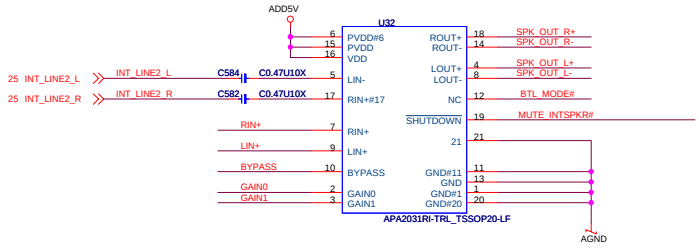


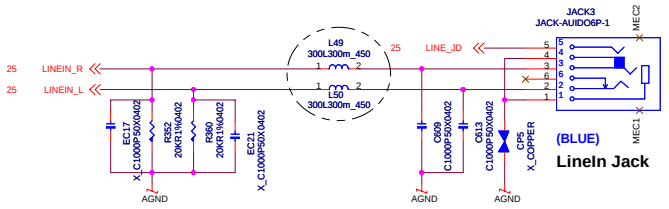
MSI	MICRO-STAR INT'L CO.,LTD.	
Title	LAN (RTL8101E)	
Size C	Document Number MS-163B1	Rev 0A
Date: Monday, April 23, 2007	Sheet 24 of 40	

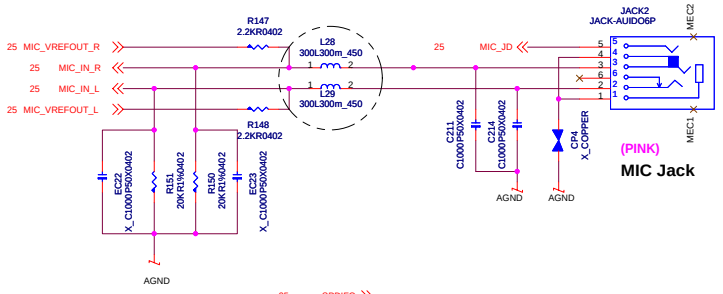


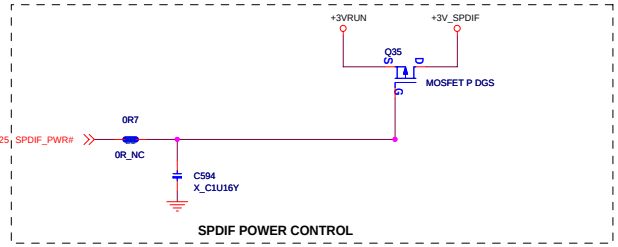
MSI	MICRO-STAR INT'L CO.,LTD		
	MS-163B1		
Size C	Document Description: Azalia CODEC (AL883)		Rev 0A
Date: Monday, April 23, 2007		Sheet 25 of 40	

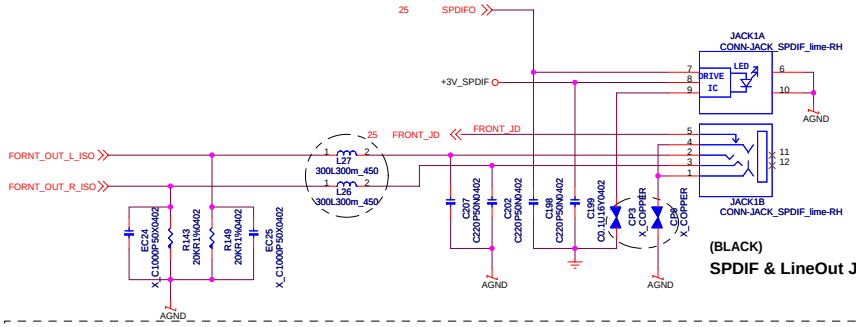


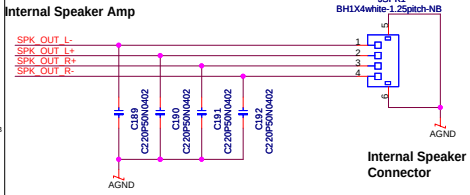


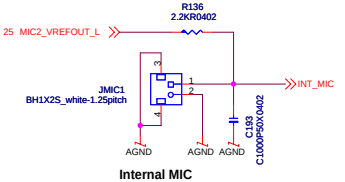


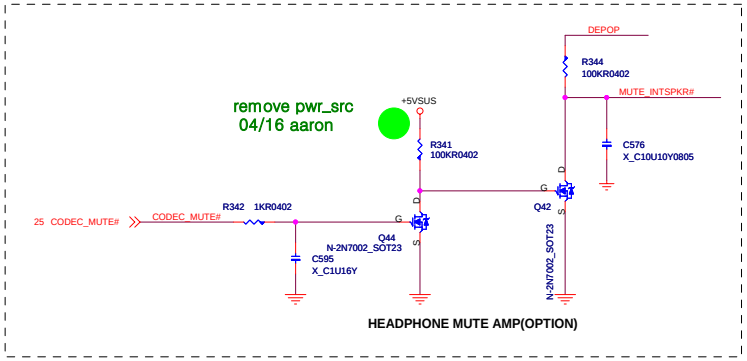


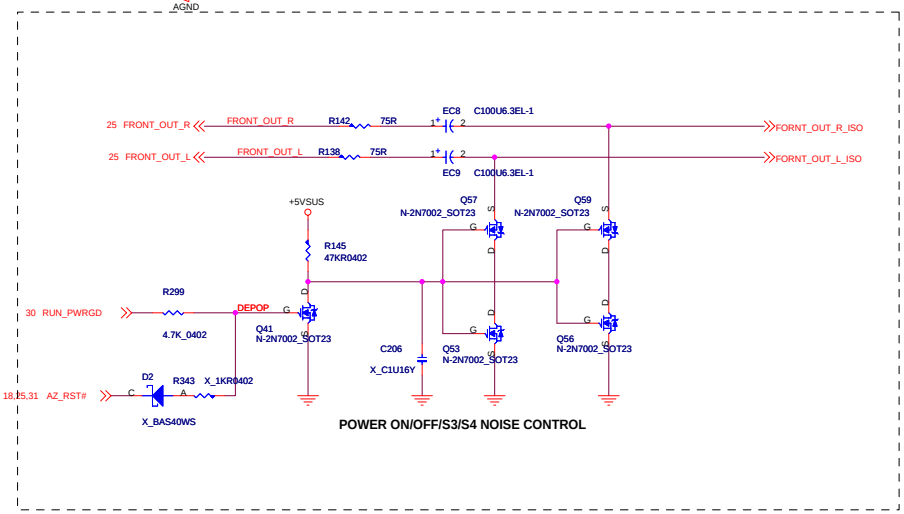






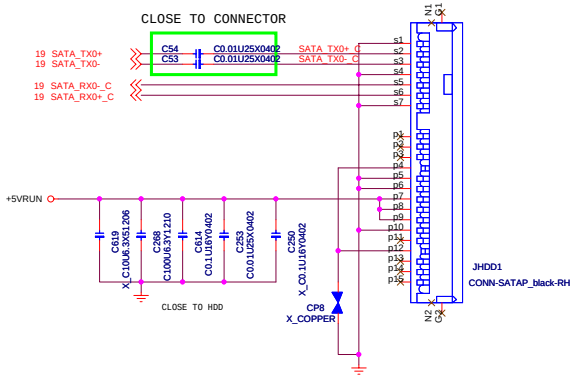


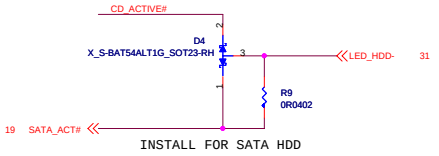




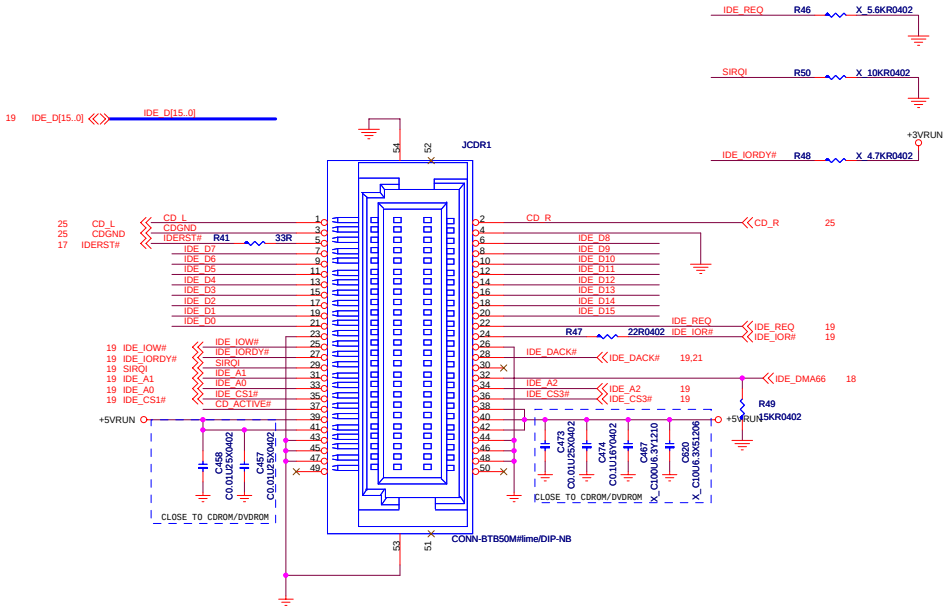
MICRO-STAR INT'L CO.,LTD	
MS-163B1	
Size: C	Document Description: Amplifier & Audio Jack
Rev: 0A	
Date: Monday, April 23, 2007	Sheet 26 of 40

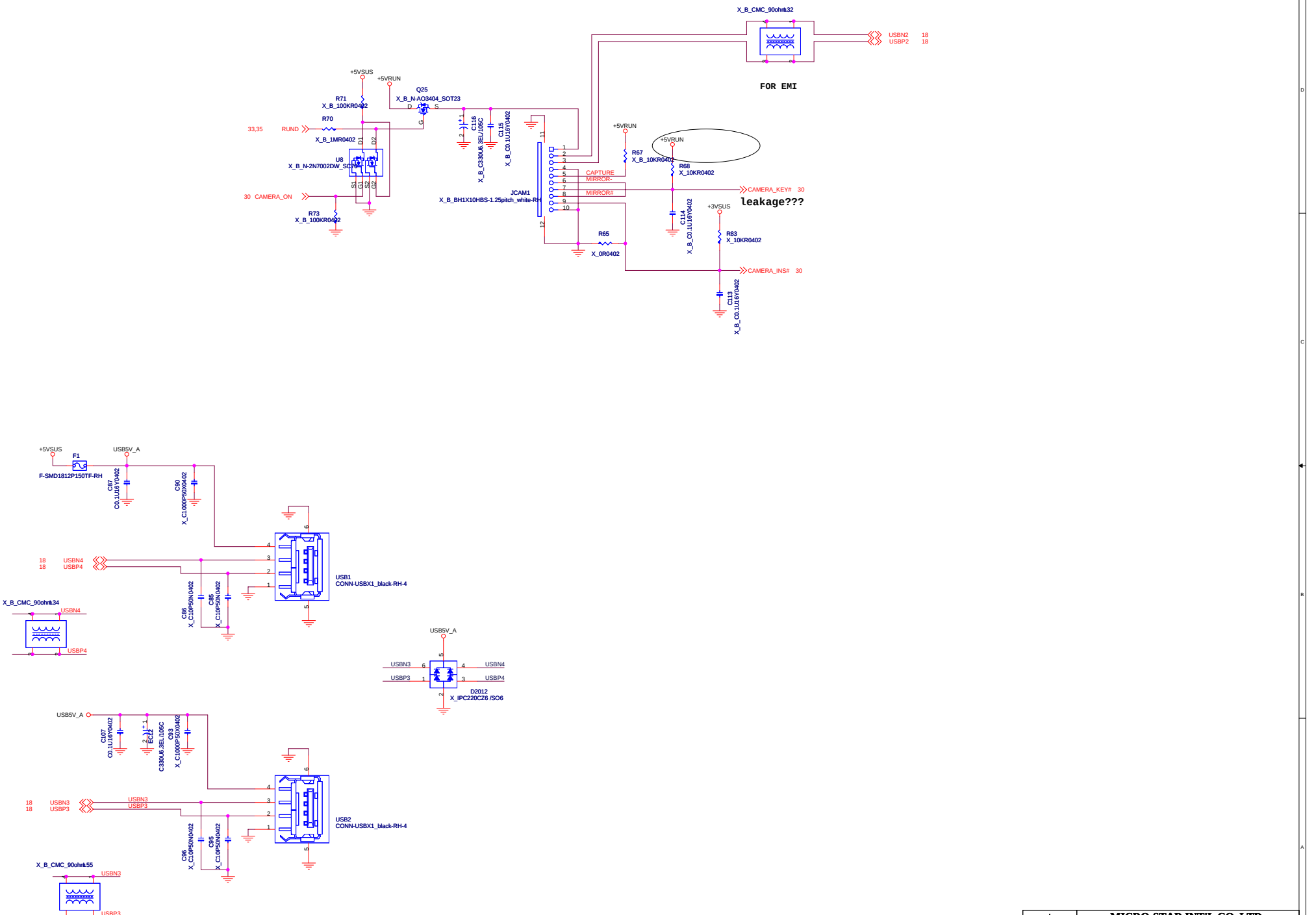
SATA HDD CONNECTOR



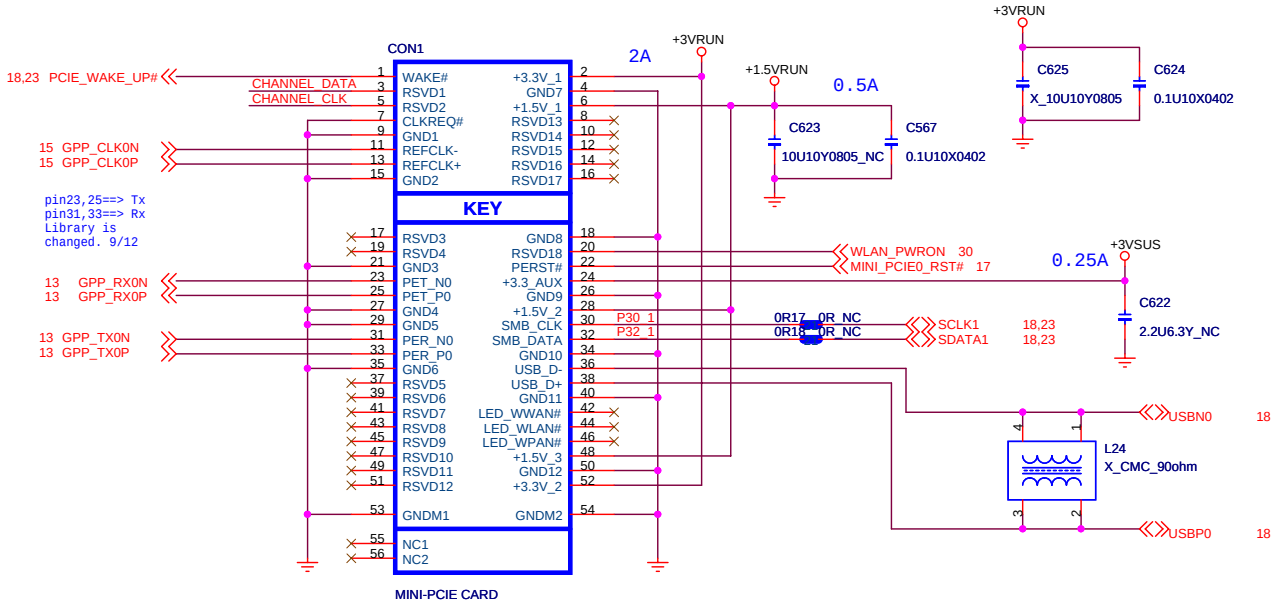


CD ROM CONNECTOR



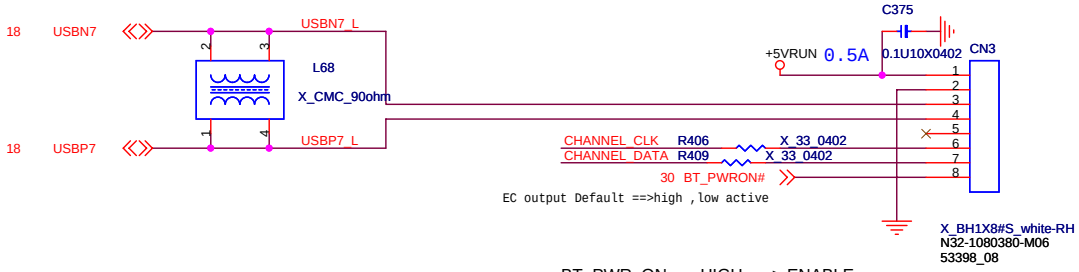


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-163B1	
Size C	Document Description: USB Connector & WEBCAM	Rev 0A
Date: Monday, April 23, 2007	Sheet 28 of 40	



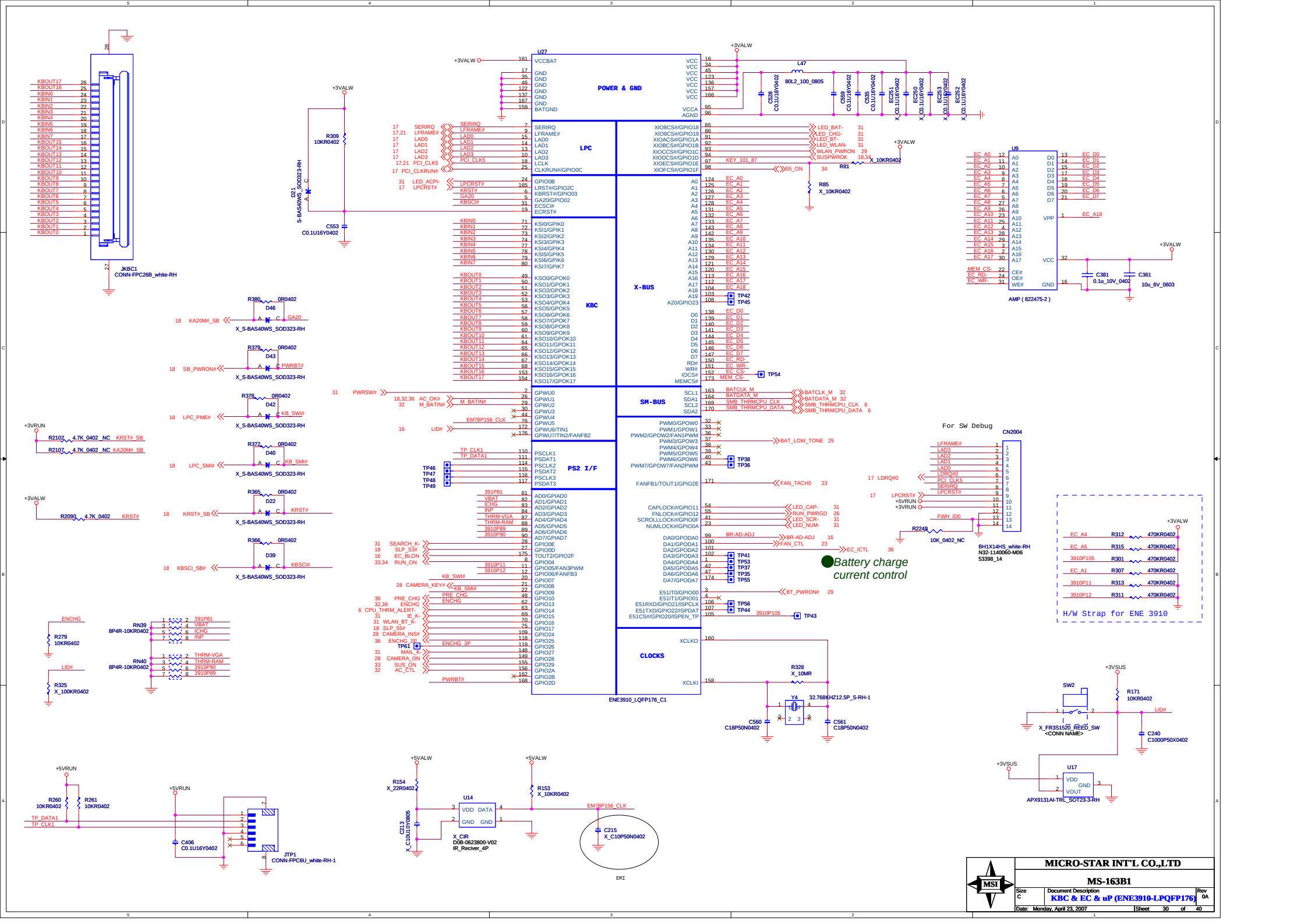
Wireless LAN

BLUETOOTH



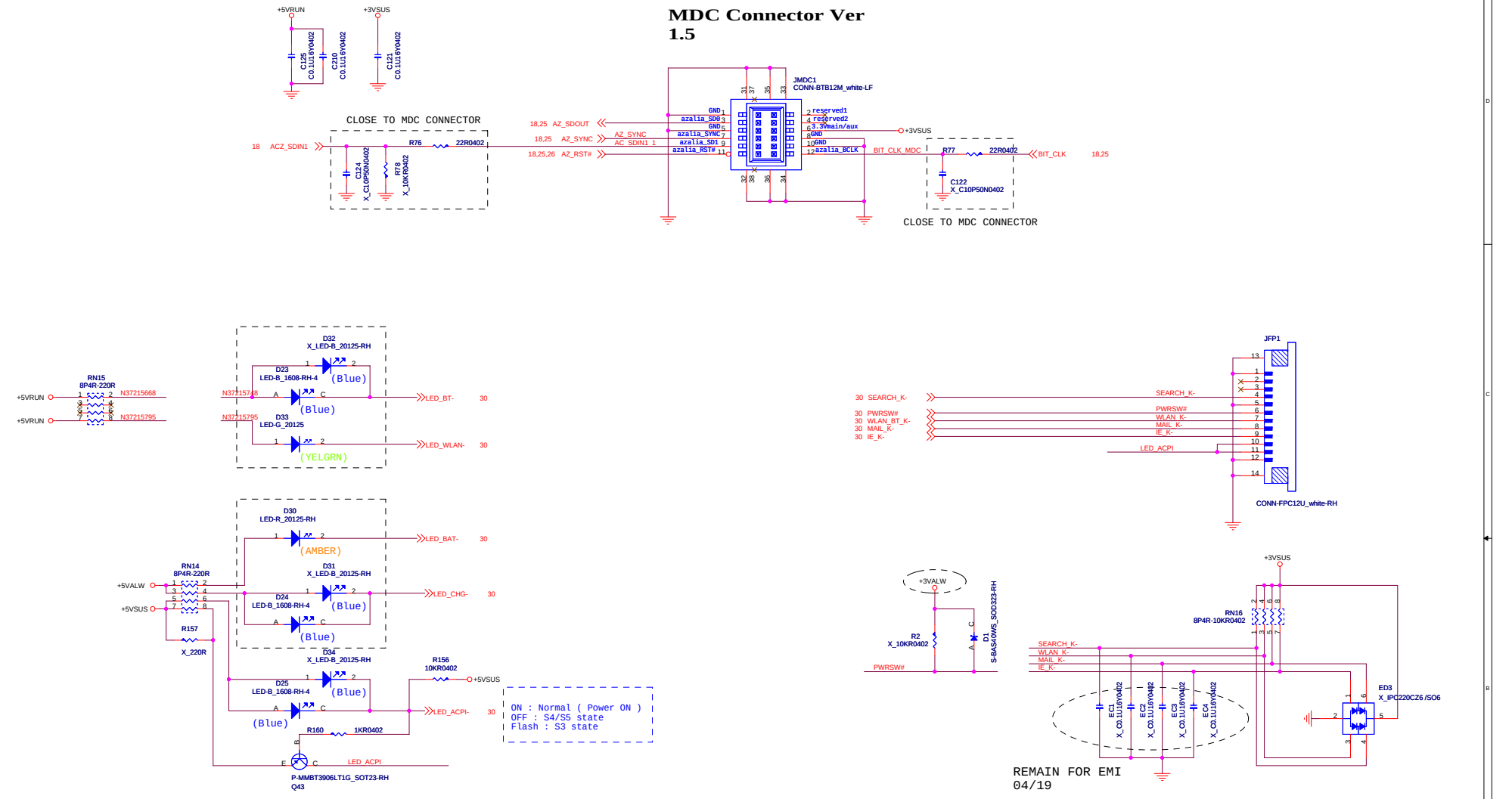
BT_PWR_ON HIGH ==> ENABLE
BT_PWR_ON LOW ==> DISENABLE

MICRO-STAR INT'L CO.,LTD		
MS-163B1		
Size: B	Document Description: Mini-PCI & WLAN/BT On/Off CTRL	Rev: 0A
Date: Monday, April 23, 2007	Sheet 29 of 40	

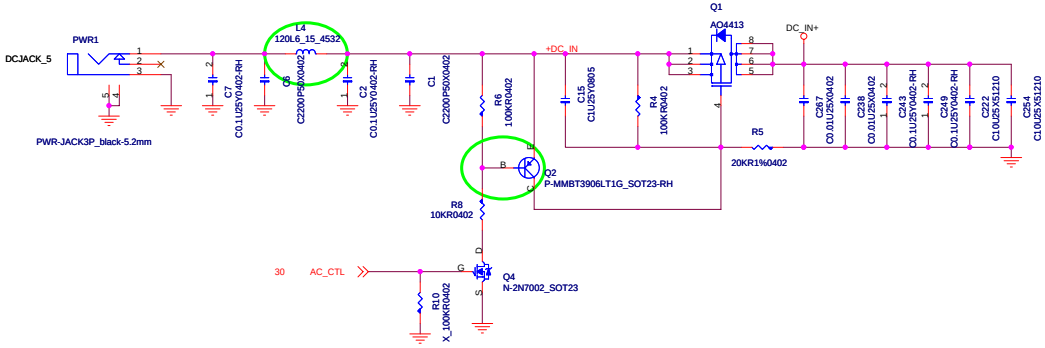


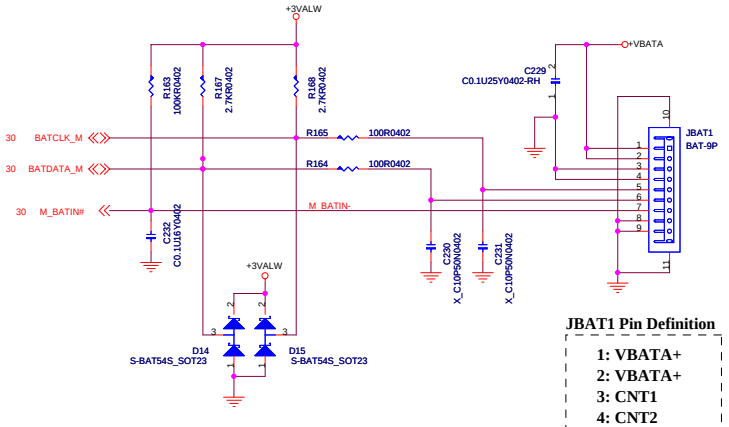
MICRO-STAR INT'L CO.,LTD	
MS-163B1	
Size: C	Document Description: KBC & EC & uP (ENE3910-LPQFP176)
Rev: 0A	
Date: Monday, April 23, 2007	Sheet 30 of 40

MDC Connector Ver 1.5



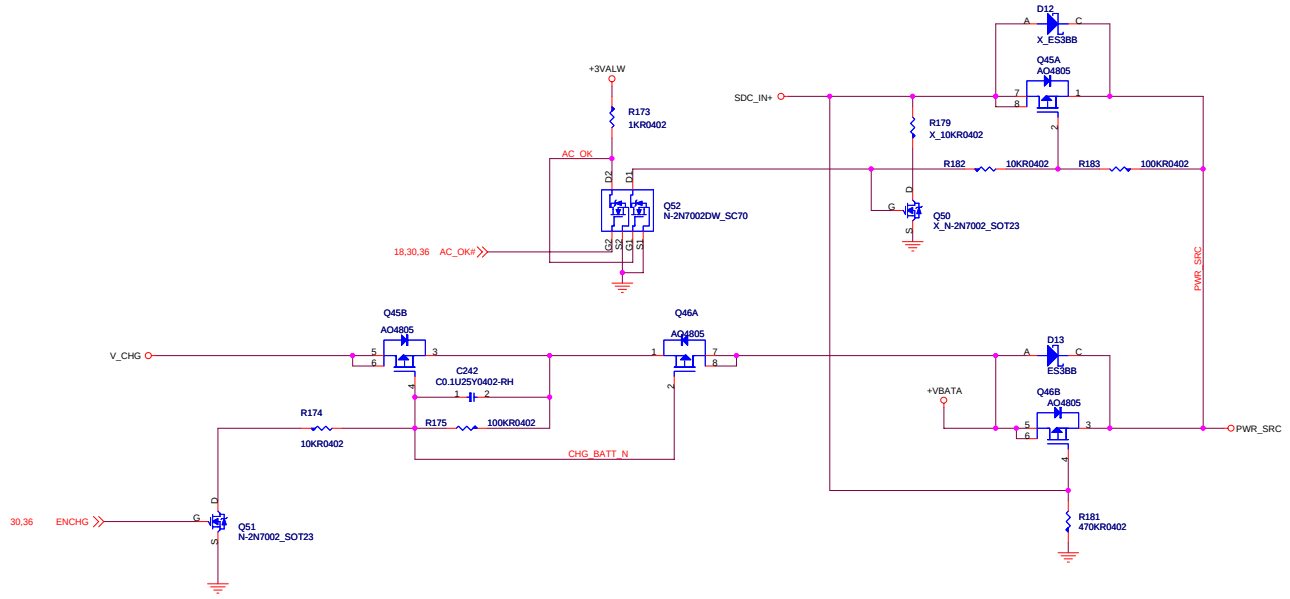
MICRO-STAR INT'L CO.,LTD	
MS-163B1	
Size: C	Document Description: MDC Connector & LED & SW
Rev: 0A	
Date: Monday, April 23, 2007	Sheet 31 of 40





JBAT1 Pin Definition

1: VBATA+
2: VBATA+
3: CNT1
4: CNT2
5: SMBCLK
6: SMBDATA
7: THERMAL
8: VBATA-
9: VBATA-
10: GND
11: GND



MICRO-STAR INT'L CO.,LTD

MS-163B1

Size	Document Description	Rev
C	Battery Select	0A

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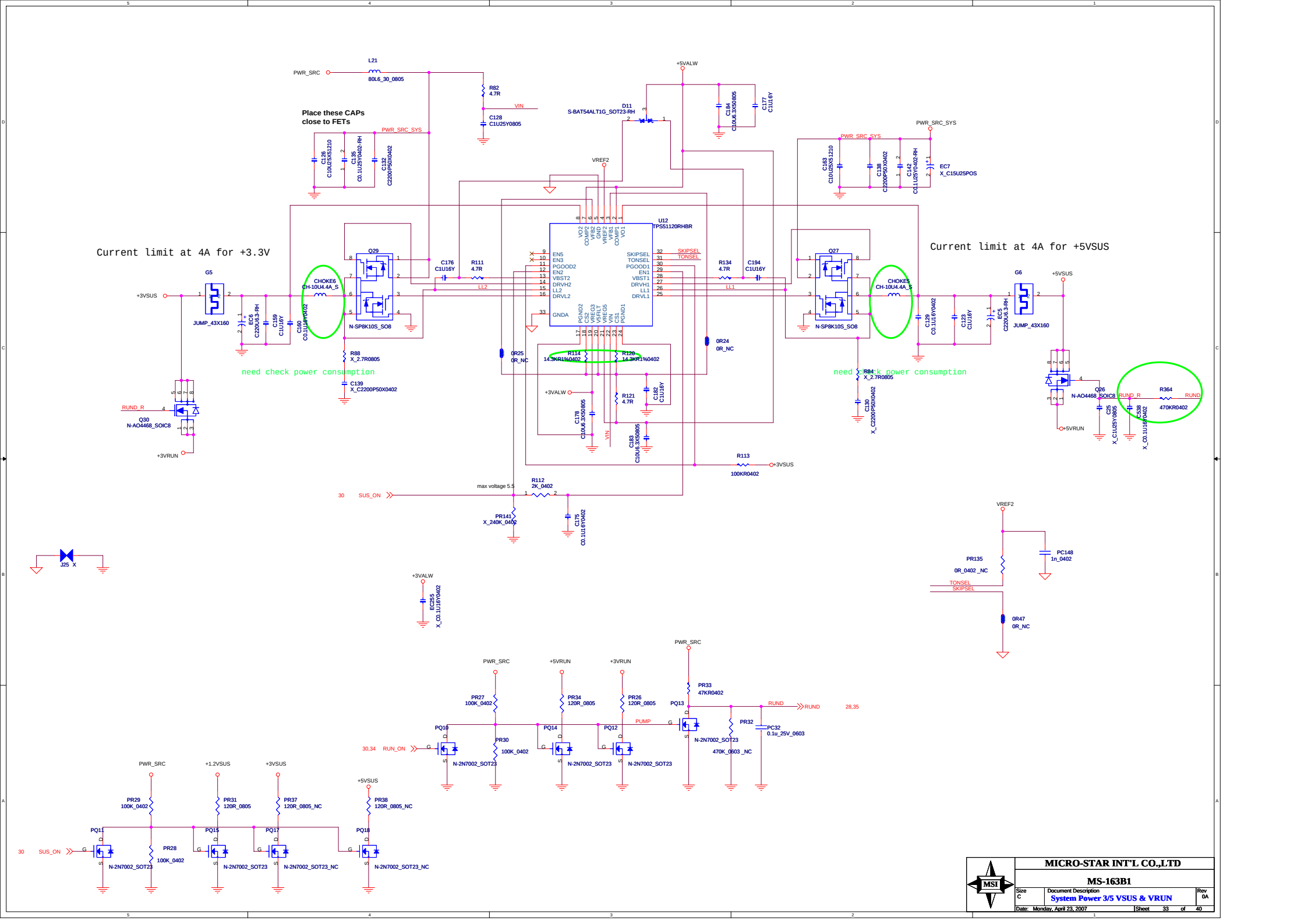
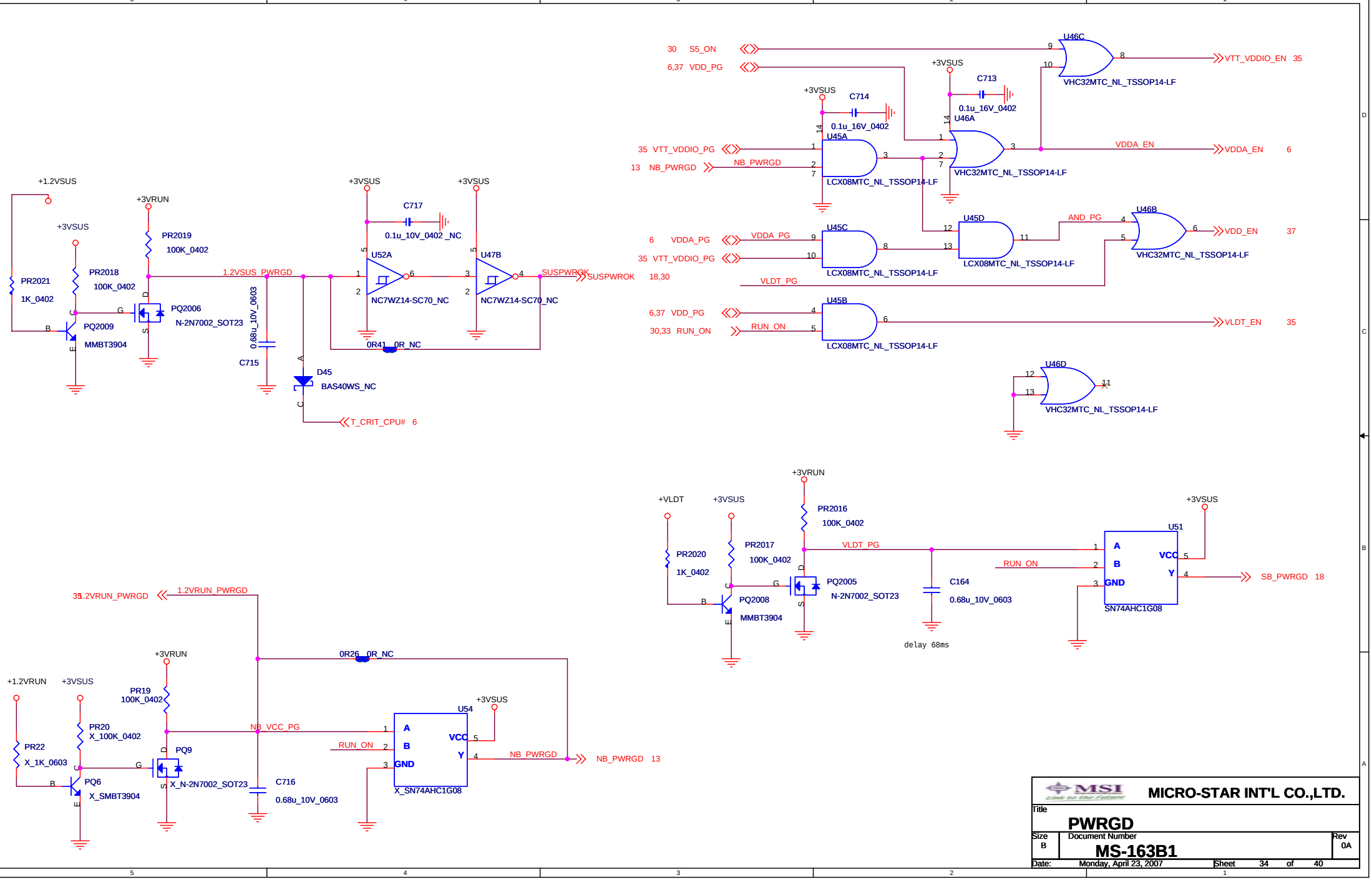
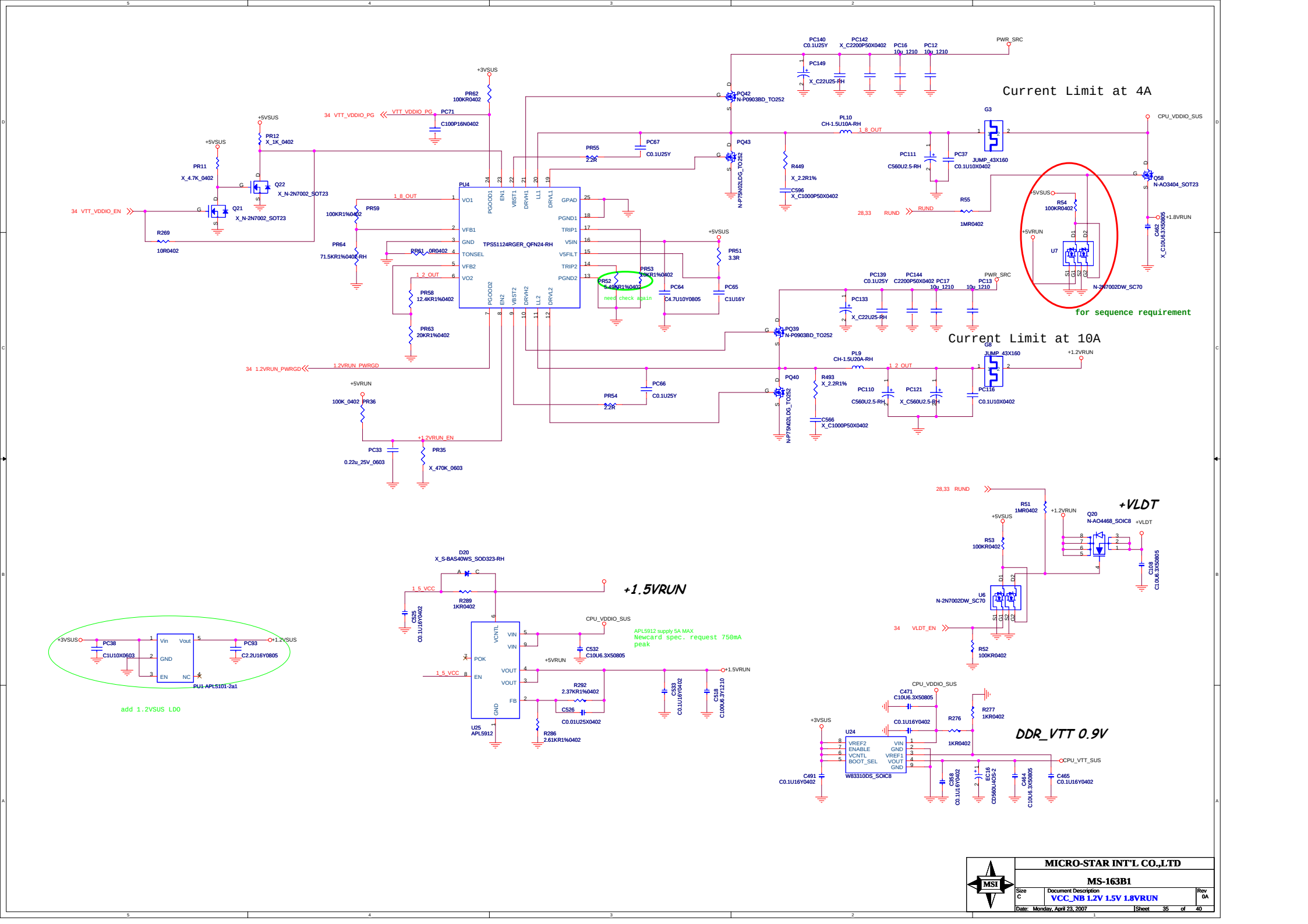

Current limit at 4A for +3.3V
Current limit at 4A for +5VSUS
Place these CAPs close to FETs
need check power consumption
need check power consumption
U12
TPS51120RHBR
Q29
Q27
G5
G6
CHOKE6
CH-10U4.4A_S
CHOKE5
CH-10U4.4A_S
N-SP8K10S_SO8
N-SP8K10S_SO8
JUMP_43X160
JUMP_43X160
Q30
N-AO4468_SOIC8
Q26
N-AO4468_SOIC8
L21
80L6_30_0805
PWR_SRC
PWR_SRC_SYS
PWR_SRC_SYS
VIN
+5VALW
+3VSUS
+5VSUS
+3VRUN
+5VRUN
+3VALW
VREF2
LL2
LL1
SKIPSEL
TONSEL
PUMP
RUND
RUND_R
RUN_ON
SUS_ON
30
28,35
max voltage 5.5
R82 4.7R
C128 C1U25Y0805
D11 S-BAT54ALT1G_SOT23-RH
C184 C10U6.3X5S0805
C177 C1U16Y
C126 C10U25X5S1210
C135 C0.1U25Y0402-RH
C132 C2200P50X0402
C163 C10U25X5S1210
C138 C2200P50X0402
C142 C0.1U25Y0402-RH
EC7 X_C15U25POS
R88 X_2.7R0805
R84 X_2.7R0805
C139 X_C2200P50X0402
C130 X_C2200P50X0402
C176 C1U16Y
R111 4.7R
R134 4.7R
C194 C1U16Y
R114 14.3KR1%0402
R120 14.3KR1%0402
R121 4.7R
C182 C1U16Y
C178 C10U6.3X5S0805
C183 C10U6.3X5S0805
0R24 0R_NC
0R25 0R_NC
R113 100KR0402
R112 2K_0402
PR141 X_240K_0402
C175 C0.1U16Y0402
C159 C1U16Y
C160 C0.1U16Y0402
EC6 C220U6.3-RH
C129 C0.1U16Y0402
C123 C1U16Y
EC5 C220U6.3-RH
C25 X_C1U25Y0805
C538 X_C0.1U16Y0402
R364 470KR0402
EC25 X_C0.1U16Y0402
PC148 1n_0402
PR135 0R_0402_NC
0R47 0R_NC
PR27 100K_0402
PR34 120R_0805
PR26 120R_0805
PR33 47KR0402
PR30 100K_0402
PR32 470K_0603_NC
PC32 0.1u_25V_0603
PQ10
PQ14
PQ12
PQ13
N-2N7002_SOT23
PR29 100K_0402
PR31 120R_0805
PR37 120R_0805_NC
PR38 120R_0805_NC
PR28 100K_0402
PQ11
PQ15
PQ17
PQ18
N-2N7002_SOT23_NC
J25 X
MICRO-STAR INT'L CO.,LTD
MS-163B1
System Power 3/5 VSUS & VRUN
Size C
Rev 0A
Date: Monday, April 23, 2007
Sheet 33 of 40



MICRO-STAR INT'L CO.,LTD.

Title	PWRGD	
Size B	Document Number MS-163B1	Rev 0A
Date: Monday, April 23, 2007	Sheet 34 of 40	


Current Limit at 4A
Current Limit at 10A
for sequence requirement
+1.5VRUN
+VLDT
DDR_VTT 0.9V
add 1.2VSUS LDO
need check again
APL5912 supply 5A MAX
Newcard spec. request 750mA peak
TPS51124RGER_QFN24-RH
MICRO-STAR INT'L CO.,LTD
MS-163B1
VCC_NB 1.2V 1.5V 1.8VRUN
Monday, April 23, 2007
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Adapter= 65W
Adapter input voltage set 17.4 Voltage
2.048/7.15*(53.6+7.15)=17.4V

Battery charge current ctronl, if this signal is used,PR100 will be modified to 0.01 ohm Aaron

3S2P: Charge current set 3 Amp
3S3P: Charge current set 4.5 Amp
Pre-charger: Charge current set 220mA

CELL GND=2 CELLS
FLOAT=3 CELLS
REFIN=4 CELLS

ICHG = (VICTL / VREFIN)x(0.75 / RS2)

ENCHG_2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

Iin = (Vcls / Vref) x(0.075 / RS1)

SET Iin MAX =3A

MICRO-STAR INT'L CO.,LTD	
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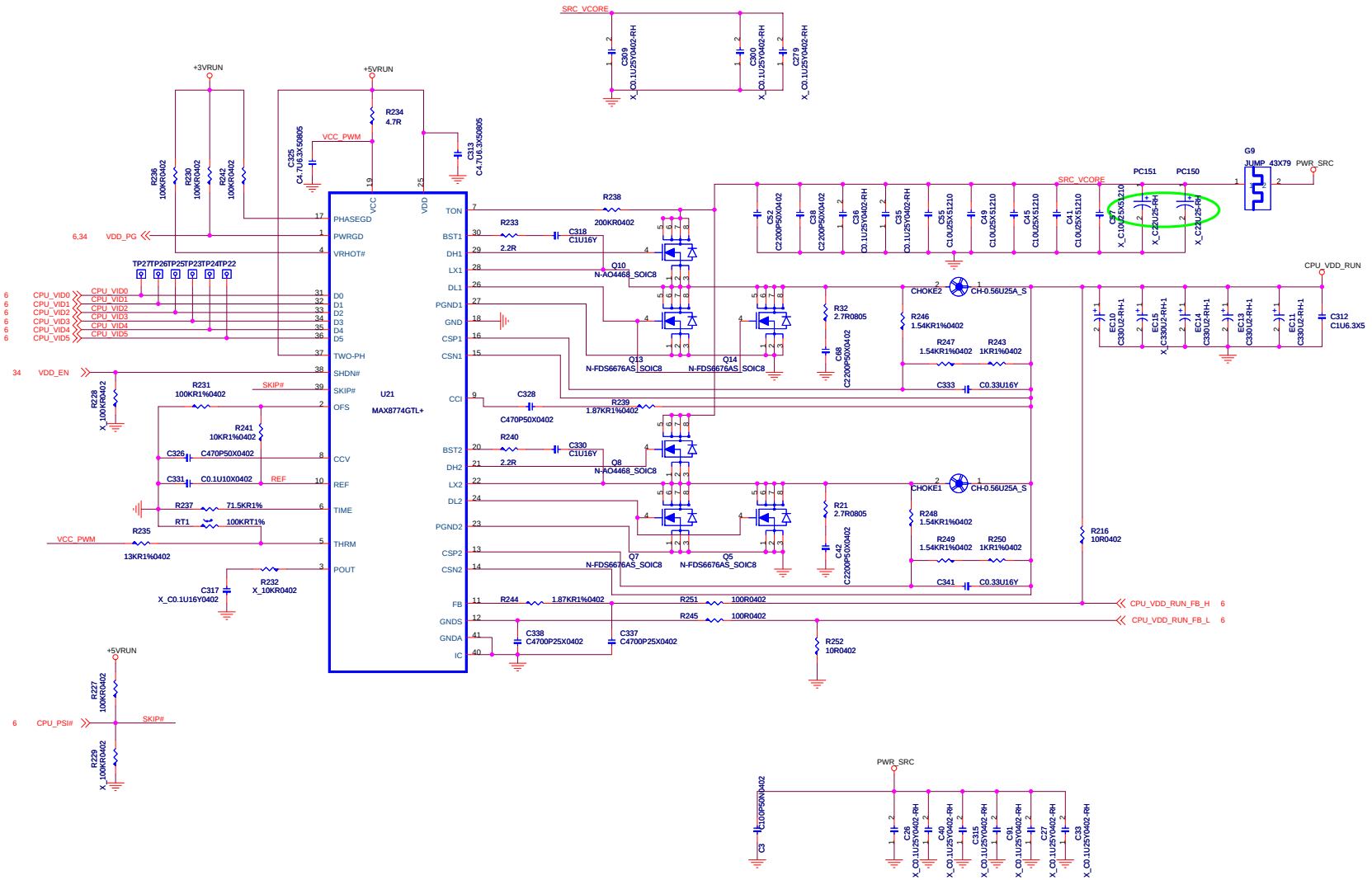
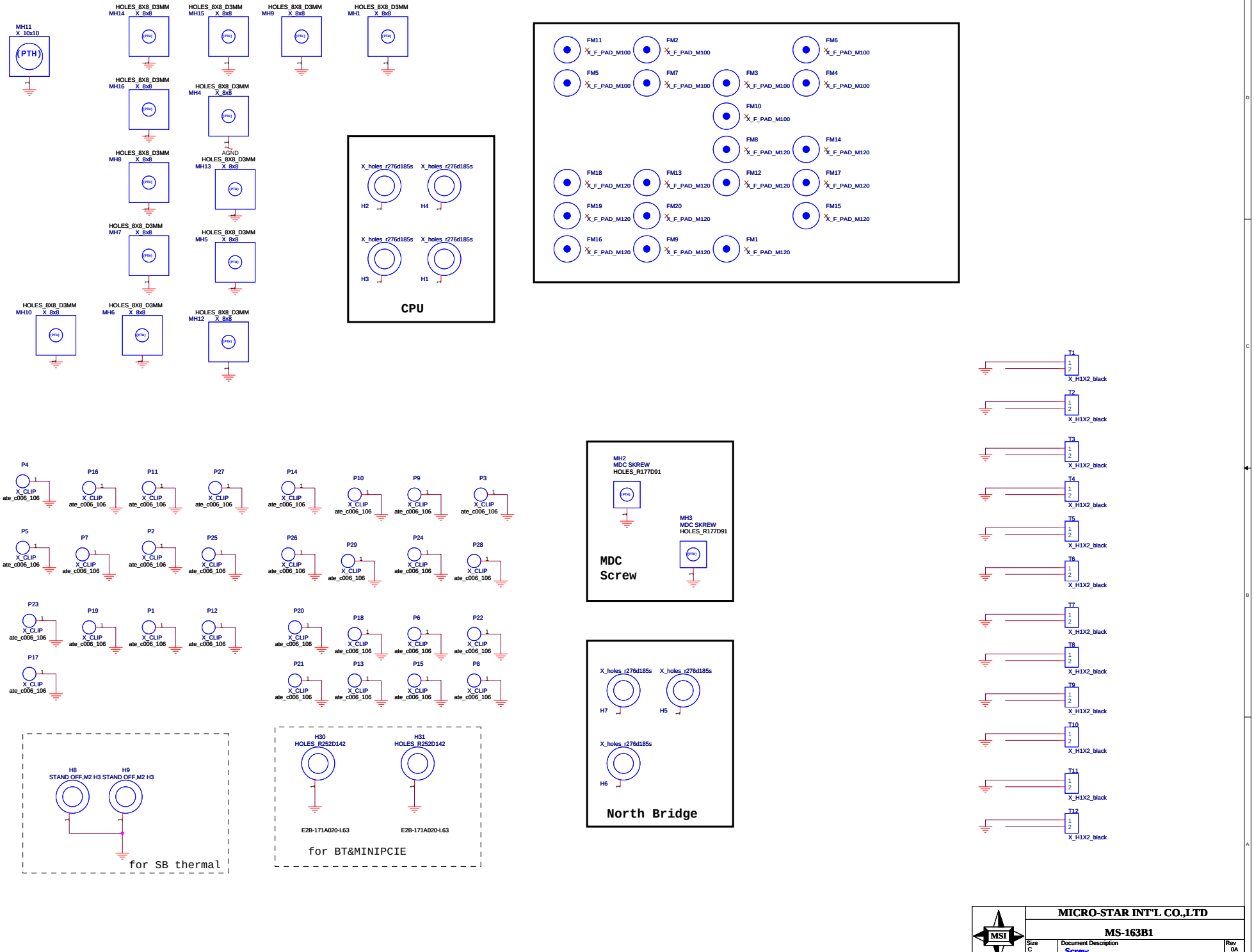
Size: C	Document Description: Battery Charger
Rev: 0A	
Date: Monday, April 23, 2007	Sheet 36 of 40



MICRO-STAR INT'L CO.,LTD		
MS-163B1		
Size: C	Document Description: CPU VCORE	Rev: 0A
Date: Monday, April 23, 2007	Sheet 37 of 40	



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
C	Screw	0A

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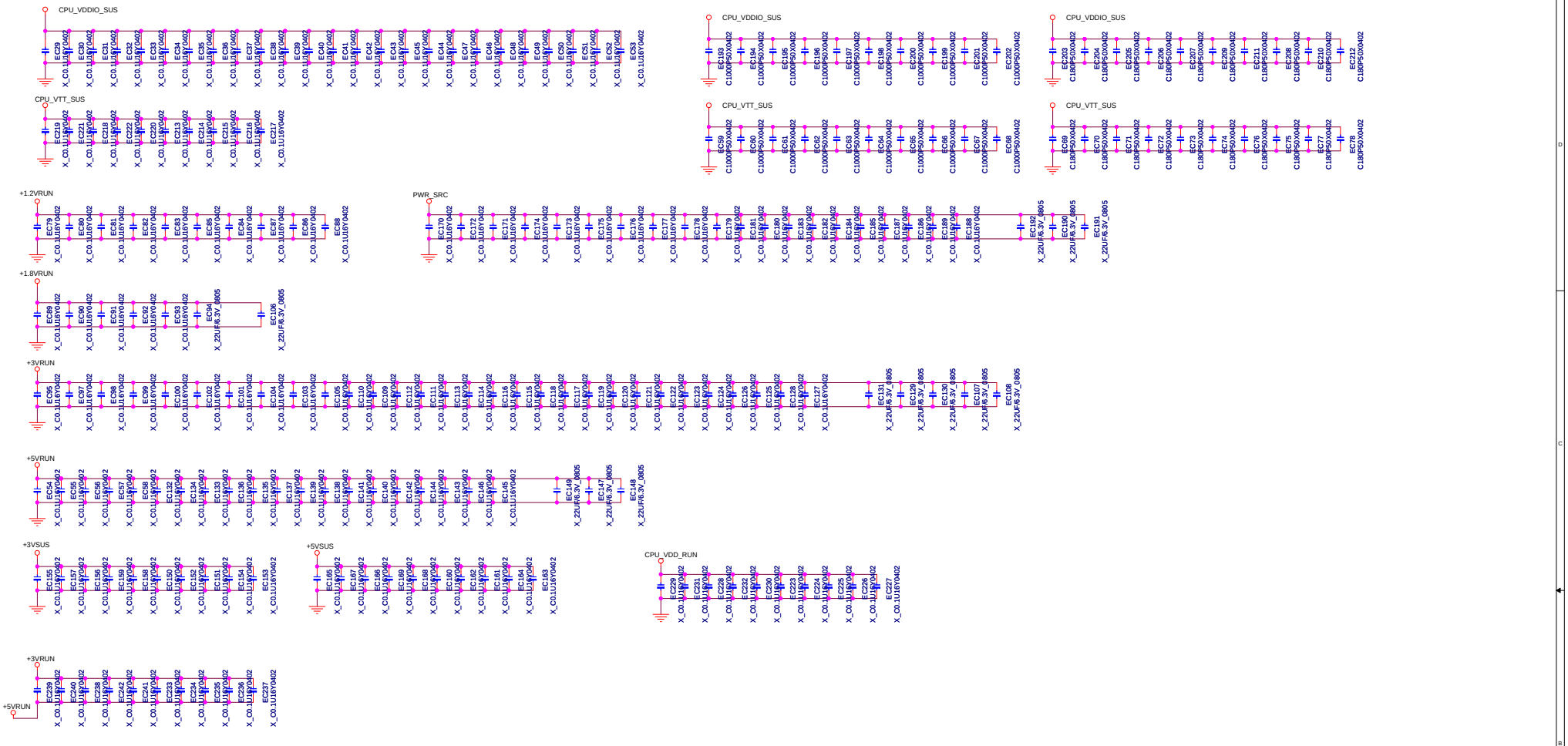

MICRO-STAR INT'L CO.,LTD			
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Size: C	Document Description: EMI Cap		Rev: 0A
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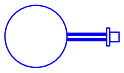
JBAT2_1



BAT-CR2032

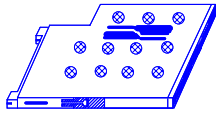
MH2_1

SCREW_M4.5X2X3 mm

MH3_1

SCREW_M4.5X2X3 mm

JPE1_1
NEW_CARD



PCI
EXPRESS 膜シ :
E23-1016010-T01

U9_1

BIOS_ROM

U9_2

BIOS_LABEL

JPE1_2

SCREW_M4.5X2X3 mm

JPE1_3

SCREW_M4.5X2X3 mm

M31-3904078-W03

JMDC1_1
MODEM_CARD

PCB1

PCB_NB16321,1.1,6L
P30-1632111-D05

JPE1_4

NEW CARD_MYLAR

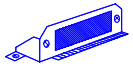
Y4_1

X_TOP SIZE Y4_MYLAR

JACK1_1

TOP SIZE LINE OUT_MYLAR

JVGA1_1



CRT SHIELDING
E2M-6323111-Y28

JVGA1_2

SCREW_4.75X4.9 mm

JVGA1_3

SCREW_4.75X4.9 mm

U9_3

MDC BACK_MYLAR

J2_1

CARDREADER_MYLAR

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Size	Document Description	Rev
C	Manual Part	0A

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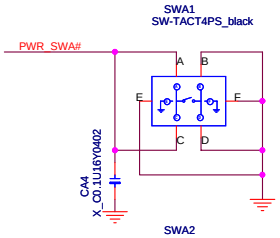

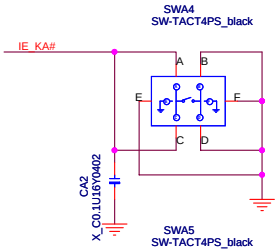

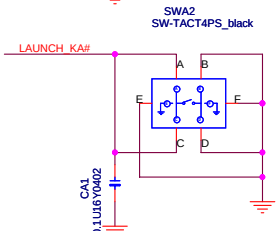

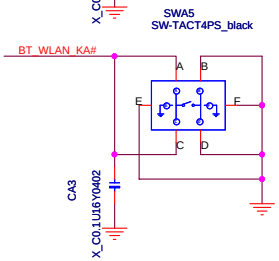

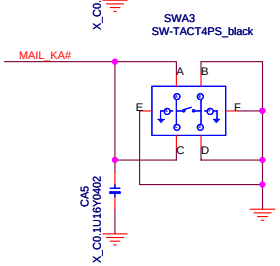

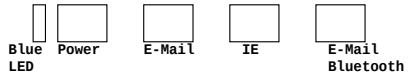

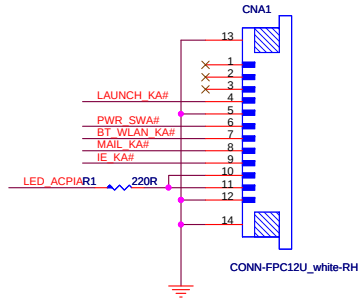

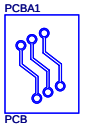

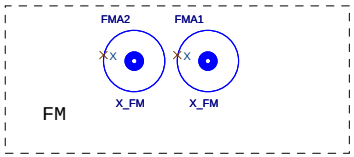

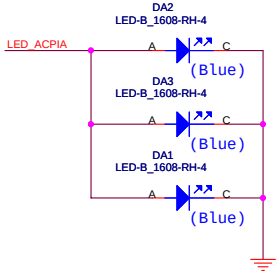

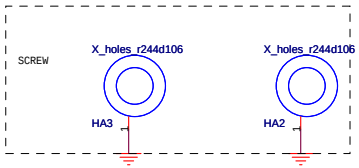

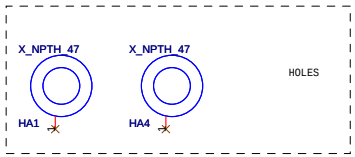

MICRO-STAR INT'L CO.,LTD

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Custom	Launch Board for MS16321	0A

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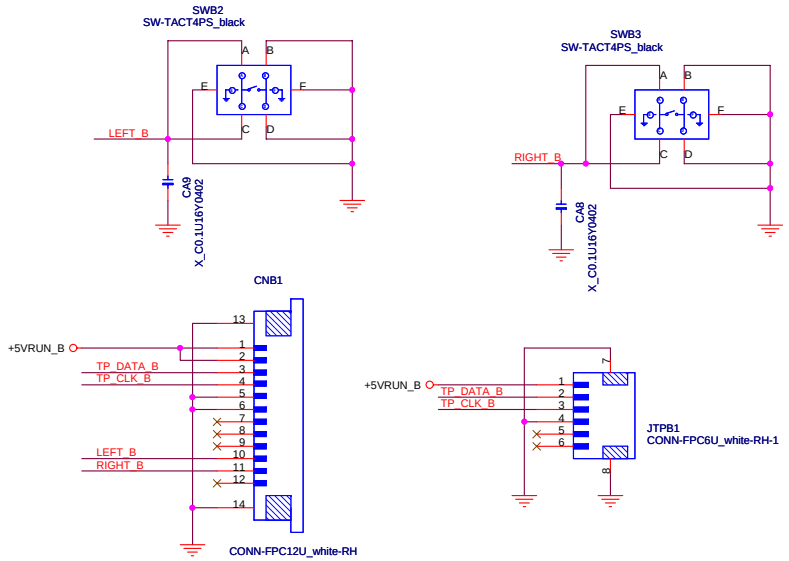

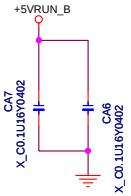

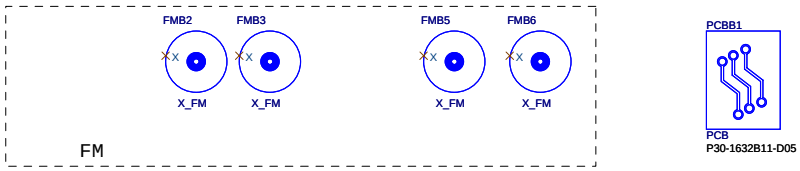

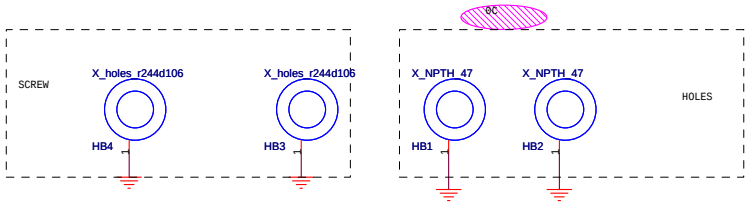

MICRO-STAR INT'L CO.,LTD		
MS-163B1		
Size: Custom	Document Description: Touch Pad Board	Rev: 0A
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